Fermi National Accelerator Laboratory

MODULE AND CRATE SUBSYSTEM TEST HARDWARE CONFIGURATIONS

HN 102

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1. General Description

The FASTBUS modules that are used in the Silicon Strip Detector (SSD) Readout System are listed below:

MAIN SYSTEM MODULES
- Postamp/Comparator (PC)
- Delay/Encoder (DE)
- Sequencer (SEQ)
- FASTBUS Smart Crate Controller (FSCC)
- Main Timing Controller (MTC)

DIAGNOSTIC MODULES
- Test Stand Module (TSM)
- Level Shifter Module(LSM)

Each of the modules listed above must be tested before being integrated into crate subsystems as shown in Figure 1. This document details the hardware configurations required to test both individual PC and DE modules and modules assembled into crate subsystems. Detailed diagnostic test information for the FSCC, MTC, and SEQ can be found in the individual hardware and software description manuals for each module. The hardware and software description documents are listed in Table I.

MODULE	HARDWARE DESC. #	SOFTWARE DESC. #	
		SINGLE BOARD	SYSTEM
FSCC	HN 96	PN 417	--
MTC	HN 98	PN 434	PN 436
SEQ	HN 99	PN 434	PN 436
PC	HN 100	PN 434	PN 436
DE	HN 101	PN 434	PN 436
TEST HARDWARE	HN 102	PN 434	PN 436

Table I: Documentation

In addition this document covers the current and appropriate fusing for each module, full crate power and difference between a SSD crate and a FASTBUS crate.

1.1 Application

The FSCC, MTC, and SEQ diagnostic tests are performed using a minimum of other module types. For example, the FSCC is tested in a stand alone mode while the MTC and SEQ need the FSCC acting as a FASTBUS master to be fully tested. The individual hardware description documents for the FSCC, MTC, and SEQ contain the hardware test configurations for those particular modules. **This document focuses on the hardware configurations required to test the PC, DE modules and the crate subsystem tests.** To simplify the description of the different hardware configurations, a series of module symbols is provided in Figure 2. These symbols are not a detailed representation of the modules front panel.The two diagnostic modules, TSM and

LSM, are used in conjunction with the FSCC, SEQ, and MTC to perform all the PC - DE tests.

All the diagnostic software used in testing the SSD readout modules is contained in EPROM that are installed in the FSCC module. These tests are stand alone requiring only a terminal. There are actually two EPROM sets (four EPROMs each set), one for system tests (SSD SYST DIAG), and one for individual module tests (SSD MOD DIAG). The user will have to swap EPROM sets (using bank 2) when changing from system to single board test unless two FSCC are available. **Please see Software Document PN 434 and PN 436 for complete software details.**

1.1.1. Packaging

The SSD readout system is package in a FASTBUS crate, but several modifications where made to accommodate the system requirements. The following are the special changes:

- The backplane is an integral unit that includes the FASTBUS segment as well as the auxiliary segment,
- The auxiliary connector of all slots are specified for readout purposes.
- The power pins +15v, -15v and 28v are allocated for +3.5v and -3.5 as required by the PC.
- A key bar is used to prevent non SSD readout modules from being plugged into the crate.

These modifications are documented in the SSD backplane specifications.

1.1.2. Physical Size

The main modules are all FASTBUS size boards. Auxiliary backplane sized modules used in individual module tests include the following:

FSCC	-	Output Port Auxiliary Backplane test module.
SEQ	-	Output Port Auxiliary Backplane test module.
DE Aux.	-	Auxiliary card for DE slot. Used for DE testing.
TSM Aux.	-	Auxiliary card for TSM slot. Used for DE testing.
SEQ Aux.	-	Auxiliary card for SEQ. Used for DE testing.

1.2 Auxiliary Backplane Module Position Pinout

The pinout of the FSCC, SEQ, PC, DE, TSM and LSM are provided in appendix A. The following is a module-slot allocation list.

SEQ	-	Slot 13.
FSCC	-	Slot 0.
DE	-	Slots 24, 22, 20, 18, 16, 14, 12, 10, 8, 6, 4, 2.

PC - Slots 25, 23, 21, 19, 17, 15, 11, 9, 7, 5, 3, 1.

1.3 Power Requirements

	+5v	-5.2v	-2v	+3.5v	-3.5v	WATTS
PC	2.74A	3.8A	4.5A	4.62A	5.63A	78.1W
DE	0.02A	14.0A	6.0A			84.9W
SEQ	9.0A	3.0A	2.0A			65.0W
FSCC	5.4A	1.2A	0.2A			33.4W
MTC	1.0A	6.0A	1.5A			58.6W
TSM	2.5A	9.0A	4.0A			67.3W
LSM	0.007A	6.5A	2.2A			38.0W

1.3.1. Module Fusing

Each FASTBUS module is both fuse and Transzorb protected. The table below shows the fusing level for each module with fuses in parallel shown in the following format; NUMBER IN PARALLEL@(FUSE VALUE).

	+5v	-5.2v	-2v	+3.5v	-3.5v
PC	1@(10A)	1@(10A)	1@(10A)	1@(10A)	1@(10A)
DE	1@(.5A)	2@(10A)	1@(10A)		
SEQ	3@(4A)	3@(2A)	1@(5A)		
FSCC	1@(10A)	1@(10A)	1@(5A)		
MTC	1@(5A)	1@(10A)	1@(5A)		
TSM	1@(4A)	2@(10A)	1@(10A)		
LSM	1@(.5A)	1@(10A)	1@(3A)		

Full Crate Power Requirements

	+5.0v	-5.2v	-2.0v	+3.5v	-3.5v
PC(12)	32.88A	45.12A	53.16A	55.44A	67.56A
DE(12)	0.24A	168.0A	72.0A		
SEQ(1)	9.0A	3.0A	2.0A		
FSCC(1)	5.4A	1.2A	0.2A		
TOTAL	47.52A	217.32A	127.36A	55.4A	67.6A

The power dissipated in the crate using the nominal voltages and currents is 2053 watts.

2. General Information

The test configurations described in this document can be divided into tests that can be performed on a FASTBUS crate (i.e. FASTBUS interface tests) and those that must be run on a SSD crate (i.e. SSD readout tests). Since the tests performed on a FASTBUS crate can also be performed on the SSD crate it will be assumed for this document that the user is always using a SSD crate. For the SSD crate the keybar will ensure that each module reside in the proper slot. Note that for the hardware configurations described in this document the only module that does not have a prespecified slot is the MTC. Since the MTC does not use the auxiliary connector it will be keyed to use any of the slots.

There are several parameters or options that have to be properly initialized. Among these there are two that require special attention; the CLK1 to CLK2 delay and the address correction parameter. The CLK1 to CLK2 delay is set by switches in the SEQ on a read only FASTBUS register. For all test using the SEQ the switches must be set to a value of 28. The address correction parameter is used to account for the difference in start time and propagation delays between different modules. This parameter essentially aligns the source and the destination. For example, when using the TSM/LS to drive the PC, data from address 0 of the TSM will not be stored in address 0 of the DE. The difference is provided to the software by the address correction parameter.

2.1 Test Hardware

The SSD readout system is based on four modules; DE, FSCC, SEQ and PC. In this section the special hardware used to test DE and PC is described. The DE test is performed with the TSM. For the PC test the TSM and LSM are used as a unit. The abbreviation TSM/LSM is used when referring to both modules.

The TSM/LSM is composed of two FASTBUS modules as shown in the block diagrams of Figure 3a and 3b. The TSM and LSM are keyed like the PC and DE, respectively. A detailed hardware description of these modules is provided in TSM/LSM Hardware Description. The TSM is composed of memory and control logic that allows the generation of 128 parallel bits of simulated hit data at the 53MHz accelerator clock rate. A different pattern can be generated every 18.9 ns. These 128 bits patterns can be used to drive the DE or to drive the LSM. The TSM implements a mode switch that selects the clock source for it's internal operation. Each of these modes is specified in such a manner that the required synchronization is provided. There are four modes (modes 0 to 3) and in this document a mode is specified for each of the hardware configurations.

The LSM module is used to convert single ended ECL data to differential with the option of selecting four possible amplitudes. These amplitudes are selected to be in the operating range of the PC inputs.

3. Single Board Test

In this section the hardware configurations required to exercise the software covered on software document PN 434 are described.

3.1 DE Test

The DE does not have a FASTBUS interface. The tested function of the module is therefore it's ability to input hit data, encode the 128 channel hit pattern into encoded hit addresses and output that data to a SEQ channel emulator or a SEQ module.

The hardware configuration in Figure 4 is used when a SEQ module is not available and testing of the DE is required. To run this test a working FSCC, SEQ and Auxiliary cards are required. The TSM is used to simulate the PC and a single input channel of the SEQ. The TSM resides in a PC module slot with the DE under test in the normal adjacent slot. The SEQ port connection is made by the auxiliary card and the backplane provides connection for the 128 data channels (this is the normal PC data connection). For this test a termination card is needed at the SEQ slot to replace the terminations provided by the SEQ. The address correction parameter for this test is set to 0.

To tests the DE the TSM is set for mode 0 or mode 1 operation, but for mode 1 a NIM clock (normally 55MHz) must be supplied for the TSM. Acceptance criteria for the DE requires that the test be run with the 55MHz clock.

Once the hardware has been properly set the user can start testing DEs. The software is menu driven with pattern data selection, looping options, stoping conditions, etc. When the test is started the appropriate bits are set on the TSM such that data transfer to the DE begins. After a delay the DE will start writing data synchronously into it's memory. If the DE and the TSM are properly synchronized the error light of the DE should be off. Synchronization problems must be fixed before proceeding with the test.

In general testing of the DE is a based on writing an event address and forcing a trigger through the TSM. After recognizing the trigger the DE encodes the event and transmits it to the TSM (SEQ channel of the TSM). The FSCC reads the event and compares it with the expected event. If errors occur they are reported to the user in a table that displays the expected data with the received data. The diagnostic software required for this test is covered in detail in document PN434.

3.2 PC Test

3.2.1. PC FASTBUS Diagnostics

When the PC diagnostics are selected from the SSD module test menu, a new menu will be displayed that includes separate detailed tests for each function of the module. To run this test a working FSCC is required. In addition there is a menu option which automatically tests all the module functions without operator intervention. If the module passes these tests without an error, then by definition the FASTBUS interface is operational. Refer to software document PN 434 for more details. The features of the module that are tested are shown below:

Geographical Addressing
Primary Address
Secondary Addressing
NTA Register
CSR00
CSR01
CSR10

Test Counter
Channel Enable/Disable
Halt Mode
Run Mode
Module I.D.
Digital-to-Analog Converters and Read back
Normal and sum channel analog inputs.

4. System Tests

The system software implements different features to perform incremental SSD readout tests. This section describes the hardware configurations that are associated with system tests covered in software document PN 436. The tests are grouped under the system tests category because they require multiple modules of the SSD readout system to be used. The are three tests covered: TSM as PC, TSM/LSM driving the input port of the PC and PC counter test.

4.1 TSM Based Test

This configuration adds the normal DE readout path to the DE tests described in section 3.1. The test setup for this configuration is shown in Figure 5. In this test the TSM replaces a PC and drives the associated DE with the data patterns specified by the user.

For this test the TSM is set for mode 2. In this mode the TSM uses CLK1 from the backplane to synchronize to the DE and it will start transmitting data when CLK1 is enable on the backplane. To check that the TSM is synchronized with the rest of the readout system the user can check the TSM front panel TC* against the DE front panel TC*. A sketch of these two signals for properly synchronized modules is shown in Figure 5. Note that DE synchronization errors will be flagged by the error led of the DE. For this test the address offset parameter is set to 0.

The encoding of an event is requested from the MTC and the encoded event is readout from the SEQ. The read back data is compared to the transmitted data and errors are reported to the user. The diagnostic software required for this test is covered in detail in document PN436.

4.2 PC Input Port Test

To test the PC input port the TSM/LSM are used with the hardware configuration shown in Figure 6. To run this test a working FSCC, SEQ, TSM/LSM and MTC are required. Note that the TSM and LSM occupy a PC and DE slot, respectively. For this test it is required that the TSM/LSM, DE, SEQ, FSCC and MTC be operational before the test is started. The TSM is set for mode 3 operation and the LSM outputs are connected to the PC inputs. In addition the TSM front panel 53MHz and SYNC are supplied by the MTC. The TSM uses the front panel clock and the sync signal to synchronize with the rest of the readout system. If the TSM has been properly initialized it will be synchronized with the rest of the SSD readout system. Note that DE synchronization is flagged by an off error LED, but for the TSM there is no such LED. TSM synchronization can be checked by referencing the front panel TC* of the DE with that of the TSM. For the cable length specified on figure 6 and for a CLK1 delay value of 39 a sketch of these two signal is

provided on the same figure. Note that the timing between these two signals changes with the CLK1 delay.

Once the software has initialized everything pattern data is generated by the TSM, converted by the LSM to the proper amplitudes, the PC discriminates and latches the input data and drives the DE. For the cable length provided the address correction parameter should be initialized to 0 and the CLK1 delay value to 39.

The encoding of an event is requested by the FSCC through the MTC and the encoded event is transmitted by the DE to the SEQ. The encoded data is read by the FSCC and compared to the test pattern. Since TSM/LSM, DE, SEQ and MTC are known to be operational, errors found are attributed to the PC under test.

4.3 PC Test Counter Test

The PC counter test is used to check the SSD readout system and to decide when a group of PCs, DEs and SEQ is functional. The test uses the internal counter of the PC to generate known data patterns. The PC is intialized such that the counter data bypasses the analog input data circuitry. This test is essentially a module integration test and is intended to be run after all the individual module tests have been successfully run and the modules are integrated into crate sub-systems. For this test the address correction parameter is set to 1.

The test is basically a module substitution tests and therefore requires that all the modules shown in Figure 7 operate correctly before tests of either the PC or the DE are attempted. The test requires that the user define the addresses of the PC to be active in the test. Note that for each PC address defined the associated DE must be present, otherwise errors will occur because encoded data is expected from a defined PC. Note that synchronization problems with the DE are reported to the MTC, but there is no report when a PC counter is out of synchronization. Because of the peculiar data patterns generated by the counter it is possible to attribute certain type of errors to a PC counter out of synchronization.

In general the test is run with a maximum of 11 DE-PC pairs which allows the MTC to reside in the same SSD crate. This minimizes communication times and increases the event testing rate. The basic test uses rolling counter with all trigger address checking (refer to software document 436) . The acceptance criteria for the crate subsystem test requires that this test run for a million events without error. Note that this criteria is for the crate subsystem and all the module used in this test must satisfy the single module test criteria.

5. Appendix A: Module Auxiliary Backplane Pinouts

Encoder Module Auxiliary Connector Pin List

(Viewed From Front of Crate-10/1/90)

C01-N/C	B01-Post/Disc Ch.00	A01-Post/Disc Ch.01
C02-GND	B02-Post/Disc Ch.02	A02-Post/Disc Ch.03
C03-N/C	B03-Post/Disc Ch.04	A03-Post/Disc Ch.05
C04-GND	B04-Post/Disc Ch.06	A04-Post/Disc Ch.07
C05-GND	B05-Post/Disc Ch.08	A05-Post/Disc Ch.09
C06-GND	B06-Post/Disc Ch.10	A06-Post/Disc Ch.11
C07-GND	B07-Post/Disc Ch.12	A07-Post/Disc Ch.13
C08-Reset	B08-Post/Disc Ch.14	A08-Post/Disc Ch.15
C09-Sync	B09-Post/Disc Ch.16	A09-Post/Disc Ch.17
C10-GND	B10-Post/Disc Ch.18	A10-Post/Disc Ch.19
C11-GND	B11-Post/Disc Ch.20	A11-Post/Disc Ch.21
C12-Sync Err	B12-Post/Disc Ch.22	A12-Post/Disc Ch.23
C13-GND	B13-Post/Disc Ch.24	A13-Post/Disc Ch.25
C14-GND	B14-Post/Disc Ch.26	A14-Post/Disc Ch.27
C15-GND	B15-Post/Disc Ch.28	A15-Post/Disc Ch.29
C16-GND	B16-Post/Disc Ch.30	A16-Post/Disc Ch.31
C17-GND	B17-Post/Disc Ch.32	A17-Post/Disc Ch.33
C18-GND	B18-Post/Disc Ch.34	A18-Post/Disc Ch.35
C19-GND	B19-Post/Disc Ch.36	A19-Post/Disc Ch.37
C20-GND	B20-Post/Disc Ch.38	A20-Post/Disc Ch.39
C21-Hit Data 0	B21-Post/Disc Ch.40	A21-Post/Disc Ch.41
C22-Hit Data 1	B22-Post/Disc Ch.42	A22-Post/Disc Ch.43
C23-GND	B23-Post/Disc Ch.44	A23-Post/Disc Ch.45
C24-Hit Data 2	B24-Post/Disc Ch.46	A24-Post/Disc Ch.47
C25-Hit Data 3	B25-Post/Disc Ch.48	A25-Post/Disc Ch.49
C26-GND	B26-Post/Disc Ch.50	A26-Post/Disc Ch.51
C27-Hit Data 4	B27-Post/Disc Ch.52	A27-Post/Disc Ch.53
C28-Hit Data 5	B28-Post/Disc Ch.54	A28-Post/Disc Ch.55
C29-GND	B29-Post/Disc Ch.56	A29-Post/Disc Ch.57
C30-Hit Data 6	B30-Post/Disc Ch.58	A30-Post/Disc Ch.59
C31-GND	B31-Post/Disc Ch.60	A31-Post/Disc Ch.61
C32-Hit Data 7	B32-Post/Disc Ch.62	A32-Post/Disc Ch.63
C33-Data VAlid	B33-Post/Disc Ch.64	A33-Post/Disc Ch.65
C34-GND	B34-Post/Disc Ch.66	A34-Post/Disc Ch.67
C35-26 MHZ Clock	B35-Post/Disc Ch.68	A35-Post/Disc Ch.69
C36-GND	B36-Post/Disc Ch.70	A36-Post/Disc Ch.71
C37-Event Address Valid	B37-Post/Disc Ch.72	A37-Post/Disc Ch.73
C38-Event Address Wrt. En.	B38-Post/Disc Ch.74	A38-Post/Disc Ch.75
C39-GND	B39-Post/Disc Ch.76	A39-Post/Disc Ch.77
C40-Event Address 0	B40-Post/Disc Ch.78	A40-Post/Disc Ch.79
C41-Event Address 1	B41-Post/Disc Ch.80	A41-Post/Disc Ch.81
C42-GND	B42-Post/Disc Ch.82	A42-Post/Disc Ch.83
C43-Event Address 2	B43-Post/Disc Ch.84	A43-Post/Disc Ch.85
C44-Event Address 3	B44-Post/Disc Ch.86	A44-Post/Disc Ch.87
C45-GND	B45-Post/Disc Ch.88	A45-Post/Disc Ch.89
C46-Event Address 4	B46-Post/Disc Ch.90	A46-Post/Disc Ch.91
C47-Event Address 5	B47-Post/Disc Ch.92	A47-Post/Disc Ch.93
C48-GND	B48-Post/Disc Ch.94	A48-Post/Disc Ch.95
C49-Event Address 6	B49-Post/Disc Ch.96	A49-Post/Disc Ch.97
C50-Event Address 7	B50-Post/Disc Ch.98	A50-Post/Disc Ch.99
C51-GND	B51-Post/Disc Ch.100	A51-Post/Disc Ch.101
C52-GND	B52-Post/Disc Ch.102	A52-Post/Disc Ch.103

C53-GND	B53-Post/Disc Ch.104	A53-Post/Disc Ch.105
C54-GND	B54-Post/Disc Ch.106	A54-Post/Disc Ch.107
C55-GND	B55-Post/Disc Ch.108	A55-Post/Disc Ch.109
C56-GND	B56-Post/Disc Ch.110	A56-Post/Disc Ch.111
C57-GND	B57-Post/Disc Ch.112	A57-Post/Disc Ch.113
C58-GND	B58-Post/Disc Ch.114	A58-Post/Disc Ch.115
C59-GND	B59-Post/Disc Ch.116	A59-Post/Disc Ch.117
C60-GND	B60-Post/Disc Ch.118	A60-Post/Disc Ch.119
C61-GND	B61-Post/Disc Ch.120	A61-Post/Disc Ch.121
C62-H53MHZ,Ø2 Clock	B62-Post/Disc Ch.122	A62-Post/Disc Ch.123
C63-L53MHZ,Ø2 Clock	B63-Post/Disc Ch.124	A63-Post/Disc Ch.125
C64-N/C	B64-Post/Disc Ch.126	A64-Post/Disc Ch.127
C65-N/C	B65-GND	A65-N/C

PC Module Auxiliary Connector Pin List

(Viewed From Front of Crate-10/1/90)

C01-H53MHZ,Ø1 Clock	B01-Post/Disc Ch.01	A01-Post/Disc Ch.00
C02-GND	B02-Post/Disc Ch.03	A02-Post/Disc Ch.02
C03-L53MHZ,Ø1 Clock	B03-Post/Disc Ch.05	A03-Post/Disc Ch.04
C04-GND	B04-Post/Disc Ch.07	A04-Post/Disc Ch.06
C05-GND	B05-Post/Disc Ch.09	A05-Post/Disc Ch.08
C06-GND	B06-Post/Disc Ch.11	A06-Post/Disc Ch.10
C07-GND	B07-Post/Disc Ch.13	A07-Post/Disc Ch.12
C08-Reset	B08-Post/Disc Ch.15	A08-Post/Disc Ch.14
C09-GND	B09-Post/Disc Ch.17	A09-Post/Disc Ch.16
C10-GND	B10-Post/Disc Ch.19	A10-Post/Disc Ch.18
C11-GND	B11-Post/Disc Ch.21	A11-Post/Disc Ch.20
C12-Analog Sum 0*	B12-Post/Disc Ch.23	A12-Post/Disc Ch.22
C13-Analog Sum 0	B13-Post/Disc Ch.25	A13-Post/Disc Ch.24
C14-Digital Sum 0*	B14-Post/Disc Ch.27	A14-Post/Disc Ch.26
C15-Digital Sum 0	B15-Post/Disc Ch.29	A15-Post/Disc Ch.28
C16-Analog Sum 1*	B16-Post/Disc Ch.31	A16-Post/Disc Ch.30
C17-Analog Sum 1	B17-Post/Disc Ch.33	A17-Post/Disc Ch.32
C18-Digital Sum 1*	B18-Post/Disc Ch.35	A18-Post/Disc Ch.34
C19-Digital Sum 1	B19-Post/Disc Ch.37	A19-Post/Disc Ch.36
C20-GND	B20-Post/Disc Ch.39	A20-Post/Disc Ch.38
C21-Analog Sum 2*	B21-Post/Disc Ch.41	A21-Post/Disc Ch.40
C22-Analog Sum 2	B22-Post/Disc Ch.43	A22-Post/Disc Ch.42
C23-Digital Sum 2*	B23-Post/Disc Ch.45	A23-Post/Disc Ch.44
C24-Digital Sum 2	B24-Post/Disc Ch.47	A24-Post/Disc Ch.46
C25-Analog Sum 3*	B25-Post/Disc Ch.49	A25-Post/Disc Ch.48
C26-Analog Sum 3	B26-Post/Disc Ch.51	A26-Post/Disc Ch.50
C27-Digital Sum 3*	B27-Post/Disc Ch.53	A27-Post/Disc Ch.52
C28-Digital Sum 3	B28-Post/Disc Ch.55	A28-Post/Disc Ch.54
C29-GND	B29-Post/Disc Ch.57	A29-Post/Disc Ch.56
C30-GND	B30-Post/Disc Ch.59	A30-Post/Disc Ch.58
C31-Analog Sum 4*	B31-Post/Disc Ch.61	A31-Post/Disc Ch.60
C32-Analog Sum 4	B32-Post/Disc Ch.63	A32-Post/Disc Ch.62
C33-Digital Sum 4*	B33-Post/Disc Ch.65	A33-Post/Disc Ch.64
C34-Digital Sum 4	B34-Post/Disc Ch.67	A34-Post/Disc Ch.66
C35-Analog Sum 5*	B35-Post/Disc Ch.69	A35-Post/Disc Ch.68
C36-Analog Sum 5	B36-Post/Disc Ch.71	A36-Post/Disc Ch.70
C37-Digital Sum 5*	B37-Post/Disc Ch.73	A37-Post/Disc Ch.72
C38-Digital Sum 5	B38-Post/Disc Ch.75	A38-Post/Disc Ch.74
C39-GND	B39-Post/Disc Ch.77	A39-Post/Disc Ch.76
C40-Analog Sum 6*	B40-Post/Disc Ch.79	A40-Post/Disc Ch.78

C41-Analog Sum 6	B41-Post/Disc Ch.81	A41-Post/Disc Ch.80
C42-Digital Sum 6*	B42-Post/Disc Ch.83	A42-Post/Disc Ch.82
C43-Digital Sum 6	B43-Post/Disc Ch.85	A43-Post/Disc Ch.84
C44-Analog Sum 7*	B44-Post/Disc Ch.87	A44-Post/Disc Ch.86
C45-Analog Sum 7	B45-Post/Disc Ch.89	A45-Post/Disc Ch.88
C46-Digital Sum 7*	B46-Post/Disc Ch.91	A46-Post/Disc Ch.90
C47-Digital Sum 7	B47-Post/Disc Ch.93	A47-Post/Disc Ch.92
C48-GND	B48-Post/Disc Ch.95	A48-Post/Disc Ch.94
C49-GND	B49-Post/Disc Ch.97	A49-Post/Disc Ch.96
C50-GND	B50-Post/Disc Ch.99	A50-Post/Disc Ch.98
C51-GND	B51-Post/Disc Ch.101	A51-Post/Disc Ch.100
C52-GND	B52-Post/Disc Ch.103	A52-Post/Disc Ch.102
C53-GND	B53-Post/Disc Ch.105	A53-Post/Disc Ch.104
C54-GND	B54-Post/Disc Ch.107	A54-Post/Disc Ch.106
C55-GND	B55-Post/Disc Ch.109	A55-Post/Disc Ch.108
C56-GND	B56-Post/Disc Ch.111	A56-Post/Disc Ch.110
C57-GND	B57-Post/Disc Ch.113	A57-Post/Disc Ch.112
C58-GND	B58-Post/Disc Ch.115	A58-Post/Disc Ch.114
C59-GND	B59-Post/Disc Ch.117	A59-Post/Disc Ch.116
C60-GND	B60-Post/Disc Ch.119	A60-Post/Disc Ch.118
C61-GND	B61-Post/Disc Ch.121	A61-Post/Disc Ch.120
C62-GND	B62-Post/Disc Ch.123	A62-Post/Disc Ch.122
C63-GND	B63-Post/Disc Ch.125	A63-Post/Disc Ch.124
C64-N/C	B64-Post/Disc Ch.127	A64-Post/Disc Ch.126
C65-N/C	B65-GND	A65-N/C

Sequencer Module Auxiliary Connector Pin List

(Viewed From Front of Crate-10/10/90)

C01-H53MHZ,Ø1 Clock, Slot 25,23,	B01-Reset	A01-H53MHZ,Ø1 Clock,Slot 11,
C02-L53MHZ,Ø1 Clock, 21,19,17,15	B02-GND	A02-L53MHZ,Ø1 Clock,9,7,5,3,1
C03-Hit Data 0, Slot 24	B03-Fiber Error	A03-Hit Data 0, Slot 2
C04-Hit Data 1, Slot 24	B04-GND	A04-Hit Data 1, Slot 2
C05-Hit Data 2, Slot 24	B05-Fiber Wait	A05-Hit Data 2, Slot 2
C06-Hit Data 3, Slot 24	B06-GND	A06-Hit Data 3, Slot 2
C07-Hit Data 4, Slot 24	B07-Fiber Clock	A07-Hit Data 4, Slot 2
C08-HIt Data 5, Slot 24	B08-GND	A08-Hit Data 5, Slot 2
C09-Hit Data 6, Slot 24	B09-Sync	A09-Hit Data 6, Slot 2
C10-Hit Data 7, Slot 24	B10-Sync Err	A10-Hit Data 7, Slot 2
C11-Data Valid, Slot 24	B11-GND	A11-Data Valid, Slot 2
C12-N/C	B12-Fiber D00	A12-N/C
C13-Hit Data 0, Slot 20	B13-GND	A13-Hit Data 0, Slot 6
C14-Hit Data 1, Slot 20	B14-Fiber D01	A14-Hit Data 1, Slot 6
C15-Hit Data 2, Slot 20	B15-GND	A15-Hit Data 2, Slot 6
C16-Hit Data 3, Slot 20	B16-Fiber D02	A16-Hit Data 3, Slot 6
C17-Hit Data 4, Slot 20	B17-GND	A17-Hit Data 4, Slot 6
C18-HIt Data 5, Slot 20	B18-Fiber D03	A18-Hit Data 5, Slot 6
C19-Hit Data 6, Slot 20	B19-GND	A19-Hit Data 6, Slot 6
C20-Hit Data 7, Slot 20	B20-Fiber D04	A20-Hit Data 7, Slot 6
C21-Data Valid, Slot 20	B21-GND	A21-Data Valid, Slot 6
C22-GND	B22-Fiber D05	A22-GND
C23-Hit Data 0, Slot 16	B23-GND	A23-Hit Data 0, Slot 10
C24-Hit Data 1, Slot 16	B24-Fiber D06	A24-Hit Data 1, Slot 10
C25-Hit Data 2, Slot 16	B25-GND	A25-Hit Data 2, Slot 10
C26-Hit Data 3, Slot 16	B26-Fiber D07	A26-Hit Data 3, Slot 10
C27-Hit Data 4, Slot 16	B27-GND	A27-Hit Data 4, Slot 10

C28-HIt Data 5, Slot 16	B28-Fiber D08	A28-Hit Data 5, Slot 10
C29-Hit Data 6, Slot 16	B29-GND	A29-Hit Data 6, Slot 10
C30-Hit Data 7, Slot 16	B30-Fiber D09	A30-Hit Data 7, Slot 10
C31-Data Valid, Slot 16	B31-GND	A31-Data Valid, Slot 10
C32-GND	B32-Fiber D10	A32-N/C
C33-Left 26 MHZ Clock	B33-GND	A33-Right 26 MHZ Clock
C34-Hit Data 0, Slot 14	B34-Fiber D11	A34-Hit Data 0, Slot 12
C35-Hit Data 1, Slot 14	B35-GND	A35-Hit Data 1, Slot 12
C36-Hit Data 2, Slot 14	B36-Fiber D12	A36-Hit Data 2, Slot 12
C37-Hit Data 3, Slot 14	B37-GND	A37-Hit Data 3, Slot 12
C38-Hit Data 4, Slot 14	B38-Fiber D13	A38-Hit Data 4, Slot 12
C39-HIt Data 5, Slot 14	B39-GND	A39-Hit Data 5, Slot 12
C40-Hit Data 6, Slot 14	B40-Fiber D14	A40-Hit Data 6, Slot 12
C41-Hit Data 7, Slot 14	B41-GND	A41-Hit Data 7, Slot 12
C42-Data Valid, Slot 14	B42-Fiber D15	A42-Data Valid, Slot 12
C43-GND	B43-GND	A43-N/C
C44-Hit Data 0, Slot 18	B44-Fiber Mux Enable	A44-Hit Data 0, Slot 8
C45-Hit Data 1, Slot 18	B45-Fiber User 2	A45-Hit Data 1, Slot 8
C46-Hit Data 2, Slot 18	B46-GND	A46-Hit Data 2, Slot 8
C47-Hit Data 3, Slot 18	B47-GND	A47-Hit Data 3, Slot 8
C48-Hit Data 4, Slot 18	B48-Event Address Valid	A48-Hit Data 4, Slot 8
C49-HIt Data 5, Slot 18	B49-Event Address Wrt En	A49-Hit Data 5, Slot 8
C50-Hit Data 6, Slot 18	B50-Event Address 0	A50-Hit Data 6, Slot 8
C51-Hit Data 7, Slot 18	B51-Event Address 1	A51-Hit Data 7, Slot 8
C52-Data Valid, Slot 18	B52-Event Address 2	A52-Data Valid, Slot 8
C53-N/C	B53-Event Address 3	A53-GND
C54-Hit Data 0, Slot 22	B54-Event Address 4	A54-Hit Data 0, Slot 4
C55-Hit Data 1, Slot 22	B55-Event Address 5	A55-Hit Data 1, Slot 4
C56-Hit Data 2, Slot 22	B56-Event Address 6	A56-Hit Data 2, Slot 4
C57-Hit Data 3, Slot 22	B57-Event Address 7	A57-Hit Data 3, Slot 4
C58-Hit Data 4, Slot 22	B58-GND	A58-Hit Data 4, Slot 4
C59-HIt Data 5, Slot 22	B59-GND	A59-Hit Data 5, Slot 4
C60-Hit Data 6, Slot 22	B60-Fiber User 1	A60-Hit Data 6, Slot 4
C61-Hit Data 7, Slot 22	B61-Fiber User 0	A61-Hit Data 7, Slot 4
C62-Data Valid, Slot 22	B62-GND	A62-Data Valid, Slot 4
C63-N/C	B63-Fiber Mux Control	A63-GND
C64-H53MHZ,Ø2 Clock, Slot 24,22,	B64-GND	A64-H53MHZ,Ø2 Clock,Slot 12,10,
C65-L53MHZ,Ø2 Clock, 20,18,16,14	B65-N/C	A65-L53MHZ,Ø2 Clock 8,6,4,2

TSM Module Auxiliary Connector Pin List

(Viewed From Front of Crate-10/9/90)

C01-H53MHZ,Ø1 Clock	B01-Post/Disc Ch.01	A01-Post/Disc Ch.00
C02-GND	B02-Post/Disc Ch.03	A02-Post/Disc Ch.02
C03-L53MHZ,Ø1 Clock	B03-Post/Disc Ch.05	A03-Post/Disc Ch.04
C04-GND	B04-Post/Disc Ch.07	A04-Post/Disc Ch.06
C05-GND	B05-Post/Disc Ch.09	A05-Post/Disc Ch.08
C06-GND	B06-Post/Disc Ch.11	A06-Post/Disc Ch.10
C07-GND	B07-Post/Disc Ch.13	A07-Post/Disc Ch.12
C08-Reset	B08-Post/Disc Ch.15	A08-Post/Disc Ch.14
C09-GND	B09-Post/Disc Ch.17	A09-Post/Disc Ch.16
C10-GND	B10-Post/Disc Ch.19	A10-Post/Disc Ch.18
C11-GND	B11-Post/Disc Ch.21	A11-Post/Disc Ch.20
C12-RES-OUT	B12-Post/Disc Ch.23	A12-Post/Disc Ch.22
C13-SYNC	B13-Post/Disc Ch.25	A13-Post/Disc Ch.24
C14-GND	B14-Post/Disc Ch.27	A14-Post/Disc Ch.26

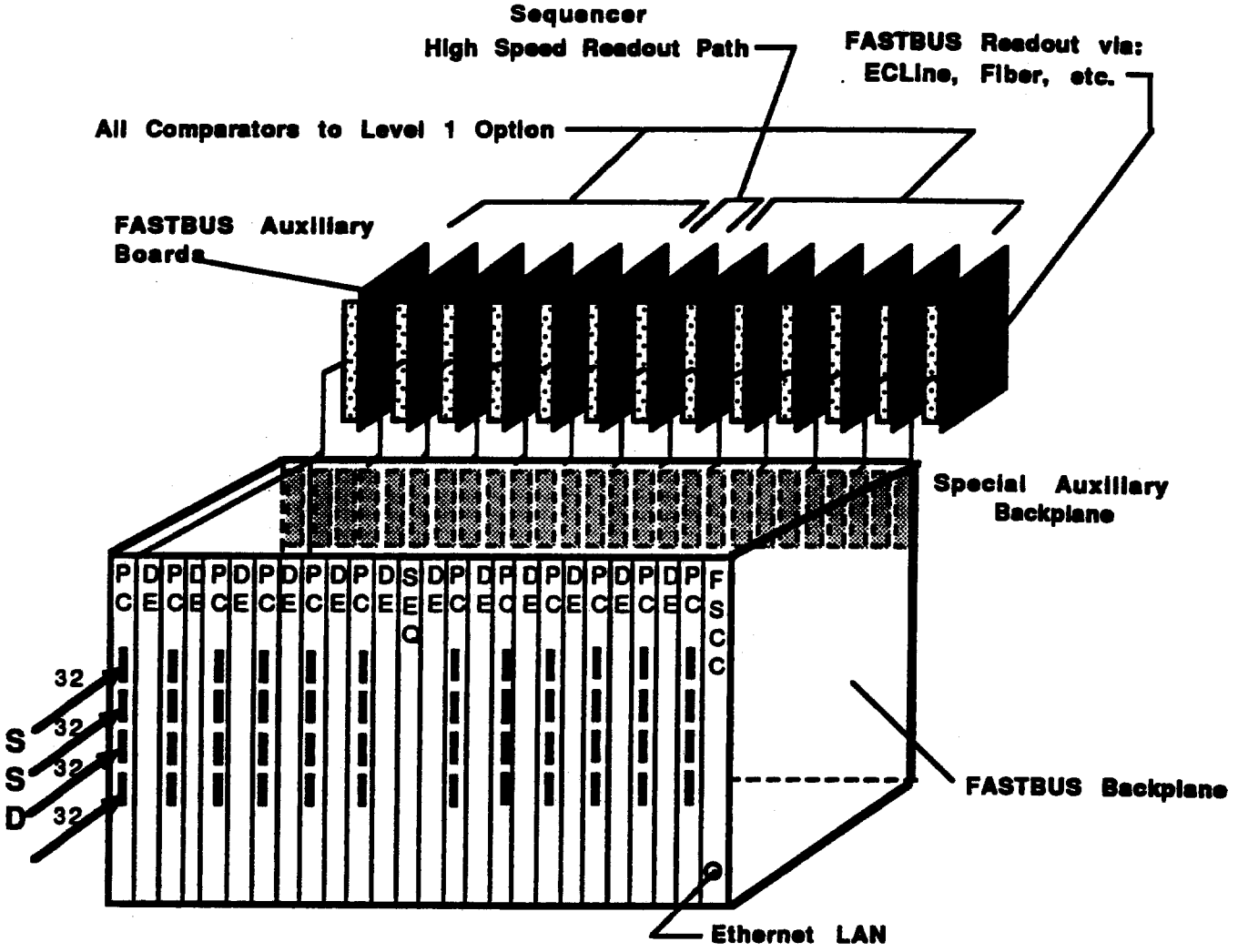
C15-SYNC-ERR	B15-Post/Disc Ch.29	A15-Post/Disc Ch.28
C16-GND	B16-Post/Disc Ch.31	A16-Post/Disc Ch.30
C17-GND	B17-Post/Disc Ch.33	A17-Post/Disc Ch.32
C18-HIT-DATA0	B18-Post/Disc Ch.35	A18-Post/Disc Ch.34
C19-HIT-DATA1	B19-Post/Disc Ch.37	A19-Post/Disc Ch.36
C20-GND	B20-Post/Disc Ch.39	A20-Post/Disc Ch.38
C21-HIT-DATA2	B21-Post/Disc Ch.41	A21-Post/Disc Ch.40
C22-HIT-DATA3	B22-Post/Disc Ch.43	A22-Post/Disc Ch.42
C23-GND	B23-Post/Disc Ch.45	A23-Post/Disc Ch.44
C24-HIT-DATA4	B24-Post/Disc Ch.47	A24-Post/Disc Ch.46
C25-HIT-DATA5	B25-Post/Disc Ch.49	A25-Post/Disc Ch.48
C26-GND	B26-Post/Disc Ch.51	A26-Post/Disc Ch.50
C27-HIT-DATA6	B27-Post/Disc Ch.53	A27-Post/Disc Ch.52
C28-HIT-DATA7	B28-Post/Disc Ch.55	A28-Post/Disc Ch.54
C29-GND	B29-Post/Disc Ch.57	A29-Post/Disc Ch.56
C30-GND	B30-Post/Disc Ch.59	A30-Post/Disc Ch.58
C31-DATA-VALID	B31-Post/Disc Ch.61	A31-Post/Disc Ch.60
C32-26MHZ(CLK3)	B32-Post/Disc Ch.63	A32-Post/Disc Ch.62
C33-GND	B33-Post/Disc Ch.65	A33-Post/Disc Ch.64
C34-EVENT-ADDR-VALID	B34-Post/Disc Ch.67	A34-Post/Disc Ch.66
C35-EVENT-WR-ENABLE	B35-Post/Disc Ch.69	A35-Post/Disc Ch.68
C36-GND	B36-Post/Disc Ch.71	A36-Post/Disc Ch.70
C37-ADDR0	B37-Post/Disc Ch.73	A37-Post/Disc Ch.72
C38-ADDR1	B38-Post/Disc Ch.75	A38-Post/Disc Ch.74
C39-GND	B39-Post/Disc Ch.77	A39-Post/Disc Ch.76
C40-ADDR2	B40-Post/Disc Ch.79	A40-Post/Disc Ch.78
C41-ADDR3	B41-Post/Disc Ch.81	A41-Post/Disc Ch.80
C42-GND	B42-Post/Disc Ch.83	A42-Post/Disc Ch.82
C43-ADDR4	B43-Post/Disc Ch.85	A43-Post/Disc Ch.84
C44-ADDR5	B44-Post/Disc Ch.87	A44-Post/Disc Ch.86
C45-GND	B45-Post/Disc Ch.89	A45-Post/Disc Ch.88
C46-ADDR6	B46-Post/Disc Ch.91	A46-Post/Disc Ch.90
C47-ADDR7	B47-Post/Disc Ch.93	A47-Post/Disc Ch.92
C48-GND	B48-Post/Disc Ch.95	A48-Post/Disc Ch.94
C49-GND	B49-Post/Disc Ch.97	A49-Post/Disc Ch.96
C50-GND	B50-Post/Disc Ch.99	A50-Post/Disc Ch.98
C51-GND	B51-Post/Disc Ch.101	A51-Post/Disc Ch.100
C52-GND	B52-Post/Disc Ch.103	A52-Post/Disc Ch.102
C53-GND	B53-Post/Disc Ch.105	A53-Post/Disc Ch.104
C54-GND	B54-Post/Disc Ch.107	A54-Post/Disc Ch.106
C55-GND	B55-Post/Disc Ch.109	A55-Post/Disc Ch.108
C56-GND	B56-Post/Disc Ch.111	A56-Post/Disc Ch.110
C57-GND	B57-Post/Disc Ch.113	A57-Post/Disc Ch.112
C58-GND	B58-Post/Disc Ch.115	A58-Post/Disc Ch.114
C59-GND	B59-Post/Disc Ch.117	A59-Post/Disc Ch.116
C60-GND	B60-Post/Disc Ch.119	A60-Post/Disc Ch.118
C61-GND	B61-Post/Disc Ch.121	A61-Post/Disc Ch.120
C62-53MHZ+	B62-Post/Disc Ch.123	A62-Post/Disc Ch.122
C63-53MHZ-	B63-Post/Disc Ch.125	A63-Post/Disc Ch.124
C64-N/C	B64-Post/Disc Ch.127	A64-Post/Disc Ch.126
C65-N/C	B65-GND	A65-N/C

Level Shifter Module Auxiliary Connector Pin List

(Viewed From Front of Crate-10/1/90)

C01-N/C	B01-Post/Disc Ch.00	A01-Post/Disc Ch.01
C02-GND	B02-Post/Disc Ch.02	A02-Post/Disc Ch.03
C03-N/C	B03-Post/Disc Ch.04	A03-Post/Disc Ch.05
C04-GND	B04-Post/Disc Ch.06	A04-Post/Disc Ch.07
C05-GND	B05-Post/Disc Ch.08	A05-Post/Disc Ch.09
C06-GND	B06-Post/Disc Ch.10	A06-Post/Disc Ch.11
C07-GND	B07-Post/Disc Ch.12	A07-Post/Disc Ch.13
C08-N/C	B08-Post/Disc Ch.14	A08-Post/Disc Ch.15
C09-N/C	B09-Post/Disc Ch.16	A09-Post/Disc Ch.17
C10-GND	B10-Post/Disc Ch.18	A10-Post/Disc Ch.19
C11-GND	B11-Post/Disc Ch.20	A11-Post/Disc Ch.21
C12-N/C	B12-Post/Disc Ch.22	A12-Post/Disc Ch.23
C13-GND	B13-Post/Disc Ch.24	A13-Post/Disc Ch.25
C14-GND	B14-Post/Disc Ch.26	A14-Post/Disc Ch.27
C15-GND	B15-Post/Disc Ch.28	A15-Post/Disc Ch.29
C16-GND	B16-Post/Disc Ch.30	A16-Post/Disc Ch.31
C17-GND	B17-Post/Disc Ch.32	A17-Post/Disc Ch.33
C18-GND	B18-Post/Disc Ch.34	A18-Post/Disc Ch.35
C19-GND	B19-Post/Disc Ch.36	A19-Post/Disc Ch.37
C20-GND	B20-Post/Disc Ch.38	A20-Post/Disc Ch.39
C21-N/C	B21-Post/Disc Ch.40	A21-Post/Disc Ch.41
C22-N/C	B22-Post/Disc Ch.42	A22-Post/Disc Ch.43
C23-GND	B23-Post/Disc Ch.44	A23-Post/Disc Ch.45
C24-N/C	B24-Post/Disc Ch.46	A24-Post/Disc Ch.47
C25-N/C	B25-Post/Disc Ch.48	A25-Post/Disc Ch.49
C26-GND	B26-Post/Disc Ch.50	A26-Post/Disc Ch.51
C27-N/C	B27-Post/Disc Ch.52	A27-Post/Disc Ch.53
C28-N/C	B28-Post/Disc Ch.54	A28-Post/Disc Ch.55
C29-GND	B29-Post/Disc Ch.56	A29-Post/Disc Ch.57
C30-N/C	B30-Post/Disc Ch.58	A30-Post/Disc Ch.59
C31-GND	B31-Post/Disc Ch.60	A31-Post/Disc Ch.61
C32-N/C	B32-Post/Disc Ch.62	A32-Post/Disc Ch.63
C33-N/C	B33-Post/Disc Ch.64	A33-Post/Disc Ch.65
C34-GND	B34-Post/Disc Ch.66	A34-Post/Disc Ch.67
C35-N/C	B35-Post/Disc Ch.68	A35-Post/Disc Ch.69
C36-GND	B36-Post/Disc Ch.70	A36-Post/Disc Ch.71
C37-N/C	B37-Post/Disc Ch.72	A37-Post/Disc Ch.73
C38-N/C	B38-Post/Disc Ch.74	A38-Post/Disc Ch.75
C39-GND	B39-Post/Disc Ch.76	A39-Post/Disc Ch.77
C40-N/C	B40-Post/Disc Ch.78	A40-Post/Disc Ch.79
C41-N/C	B41-Post/Disc Ch.80	A41-Post/Disc Ch.81
C42-GND	B42-Post/Disc Ch.82	A42-Post/Disc Ch.83
C43-N/C	B43-Post/Disc Ch.84	A43-Post/Disc Ch.85
C44-N/C	B44-Post/Disc Ch.86	A44-Post/Disc Ch.87
C45-GND	B45-Post/Disc Ch.88	A45-Post/Disc Ch.89
C46-N/C	B46-Post/Disc Ch.90	A46-Post/Disc Ch.91
C47-N/C	B47-Post/Disc Ch.92	A47-Post/Disc Ch.93
C48-GND	B48-Post/Disc Ch.94	A48-Post/Disc Ch.95
C49-N/C	B49-Post/Disc Ch.96	A49-Post/Disc Ch.97
C50-N/C	B50-Post/Disc Ch.98	A50-Post/Disc Ch.99
C51-GND	B51-Post/Disc Ch.100	A51-Post/Disc Ch.101
C52-GND	B52-Post/Disc Ch.102	A52-Post/Disc Ch.103
C53-GND	B53-Post/Disc Ch.104	A53-Post/Disc Ch.105
C54-GND	B54-Post/Disc Ch.106	A54-Post/Disc Ch.107
C55-GND	B55-Post/Disc Ch.108	A55-Post/Disc Ch.109
C56-GND	B56-Post/Disc Ch.110	A56-Post/Disc Ch.111

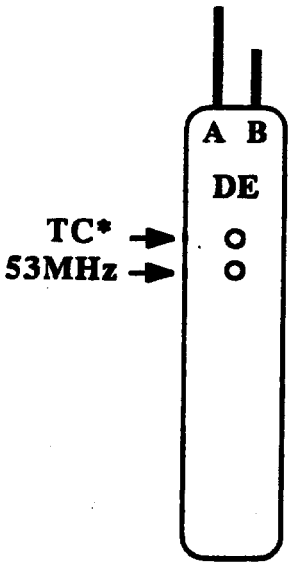
C57-GND	B57-Post/Disc Ch.112	A57-Post/Disc Ch.113
C58-GND	B58-Post/Disc Ch.114	A58-Post/Disc Ch.115
C59-GND	B59-Post/Disc Ch.116	A59-Post/Disc Ch.117
C60-GND	B60-Post/Disc Ch.118	A60-Post/Disc Ch.119
C61-GND	B61-Post/Disc Ch.120	A61-Post/Disc Ch.121
C62-N/C	B62-Post/Disc Ch.122	A62-Post/Disc Ch.123
C63-N/C	B63-Post/Disc Ch.124	A63-Post/Disc Ch.125
C64-N/C	B64-Post/Disc Ch.126	A64-Post/Disc Ch.127
C65-N/C	B65-GND	A65-N/C



SINGLE CRATE SUBSYSTEM (1536 CHANNELS)

PC - POSTAMP/COMPARATOR
DE - DELAY/ENCODER
SEQ - SEQUENCER
FSCC - FASTBUS SMART CRATE CONTROLLER

Figure 1

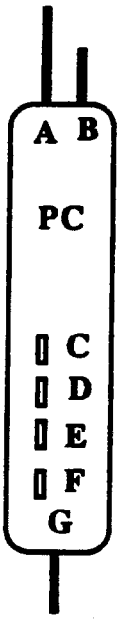


Connection:

A : 128 Hit Data.
B : Sequencer Port.

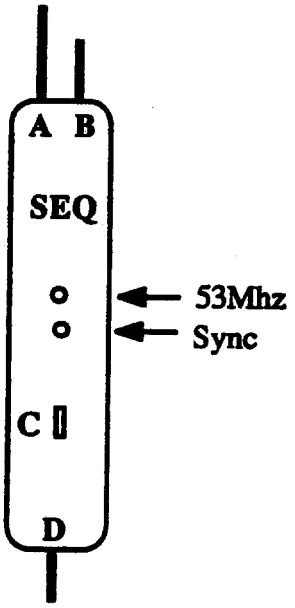
Connection:

A : 128 Input Data
B->E : 128 Diff. Output Data.



Connection:

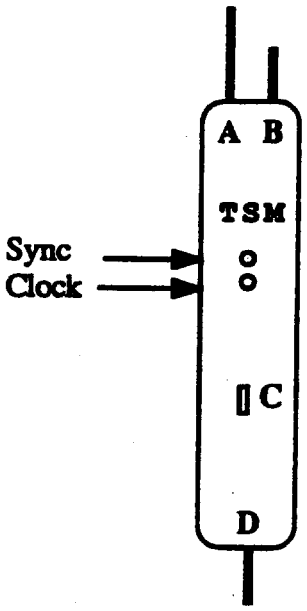
A : 128 Discriminated Output Data.
B : Sequencer Port.
C->F : 128 Differential Inputs Data.
G : FASTBUS Port.



Connection:

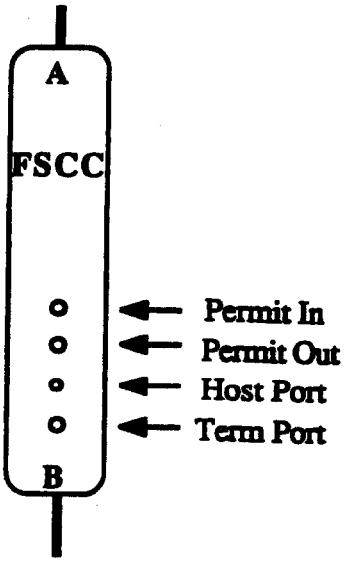
A : SSD Readout and Control.
B : Auxiliary Port Event Readout.
C : SEQ/MTC Control and Status.
D : FASTBUS Port.

Figure 2a: Module Symbols



Connection:

A - 128 Out Data.
B - Sequencer Port.
C - Fiber Receiver.
D - FASTBUS Port.



Connection:

A - Auxiliary Readout Port.
B - FASTBUS Port.

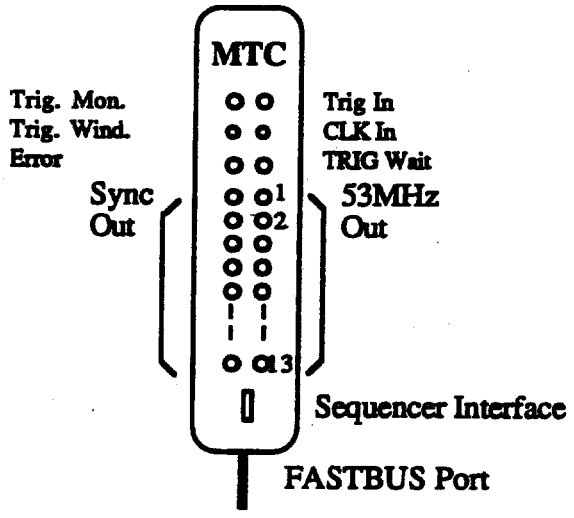


Figure 2b: Module Symbols

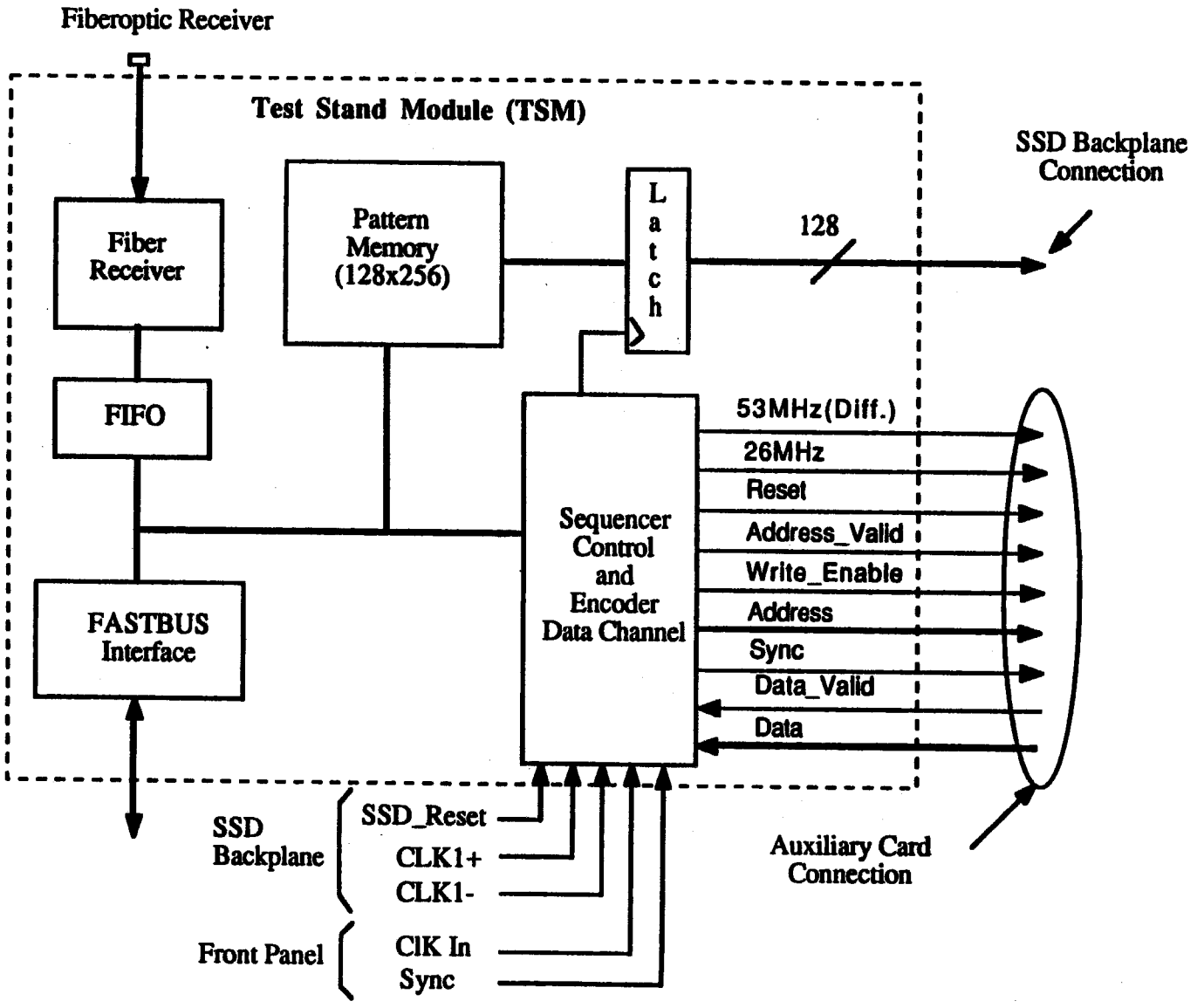
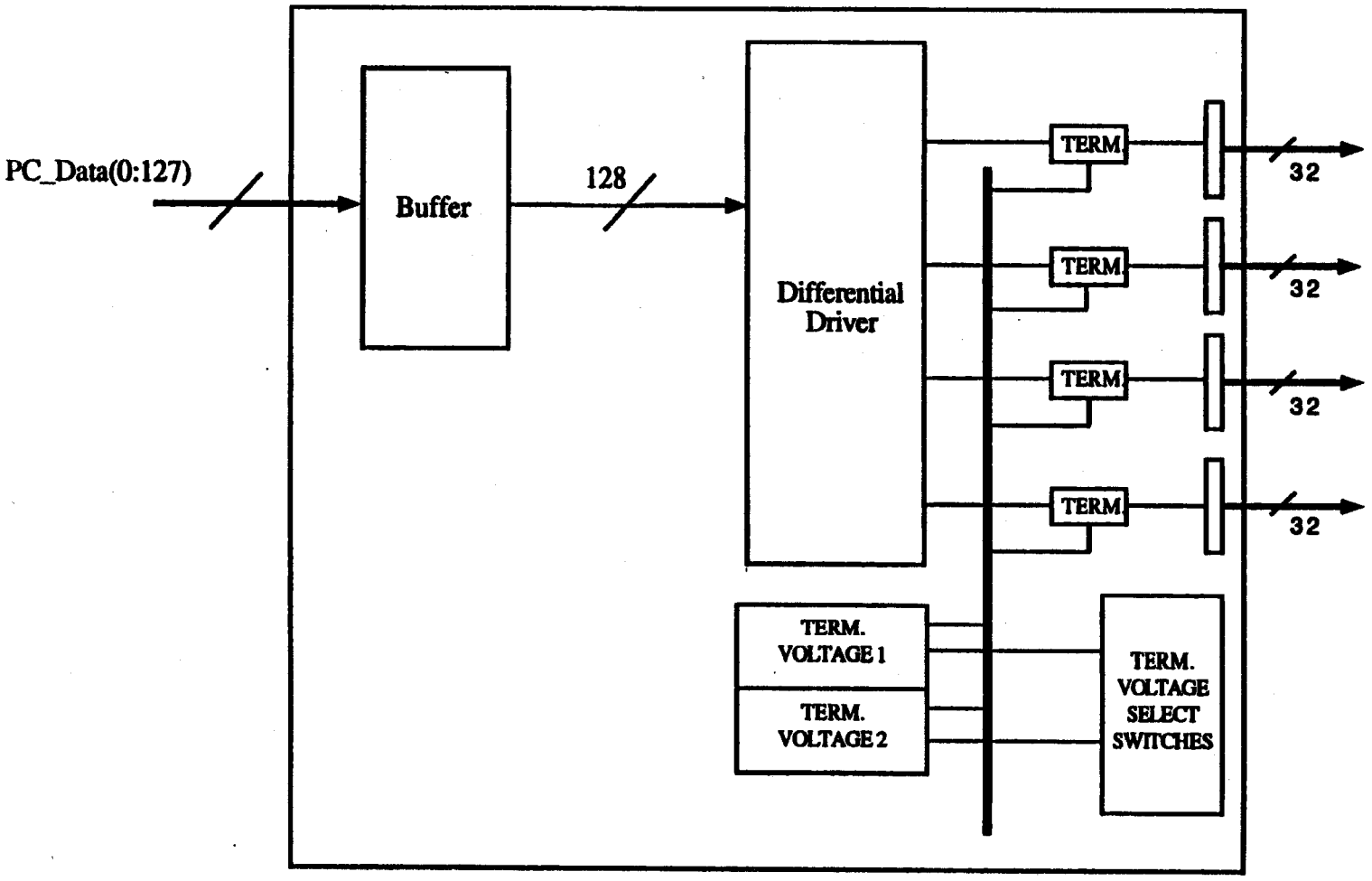


Figure 3a: TSM Block Diagram



Note: LS uses PC slot key.

Figure 3b: Level Shifter Block Diagram

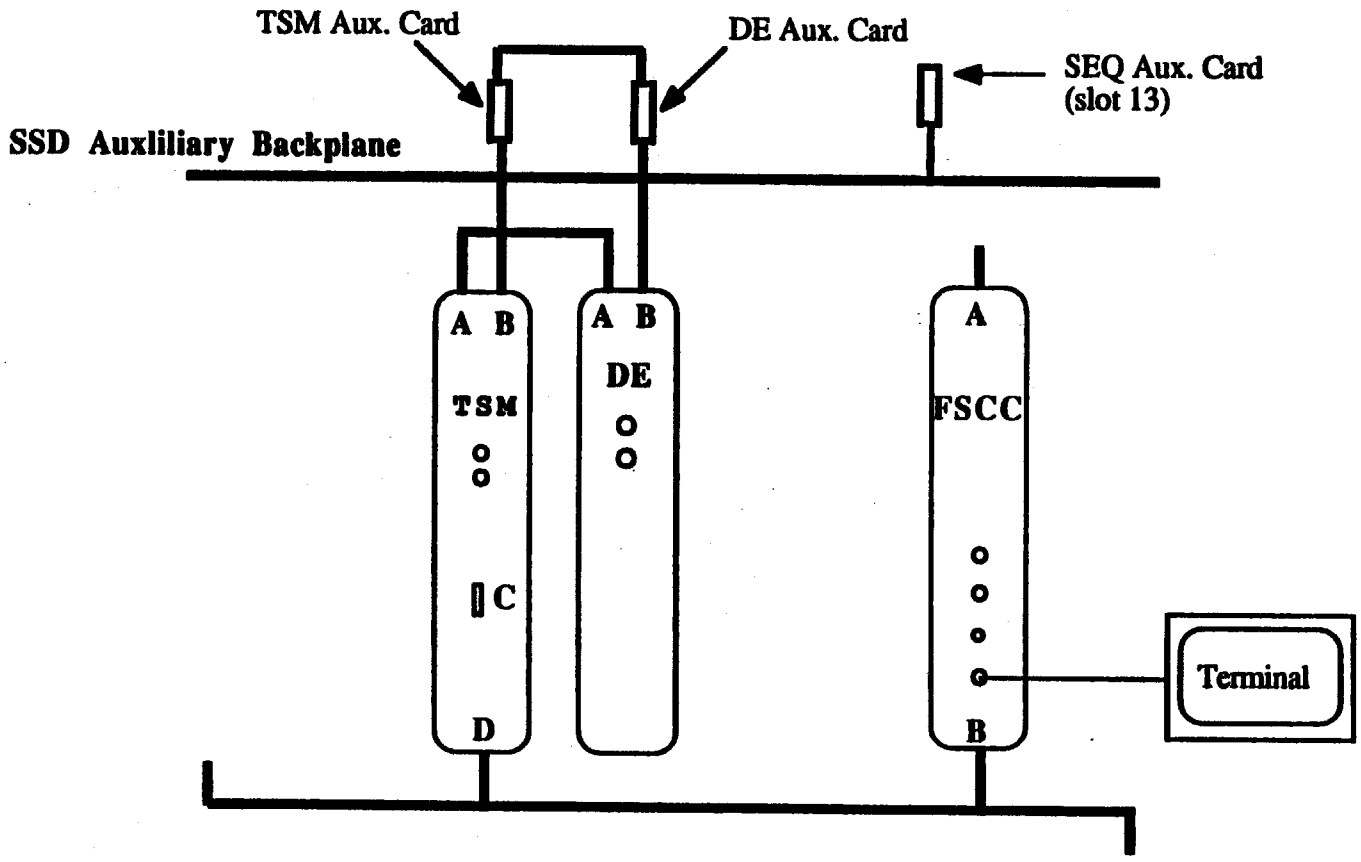


Figure 4: DE Testing with TSM

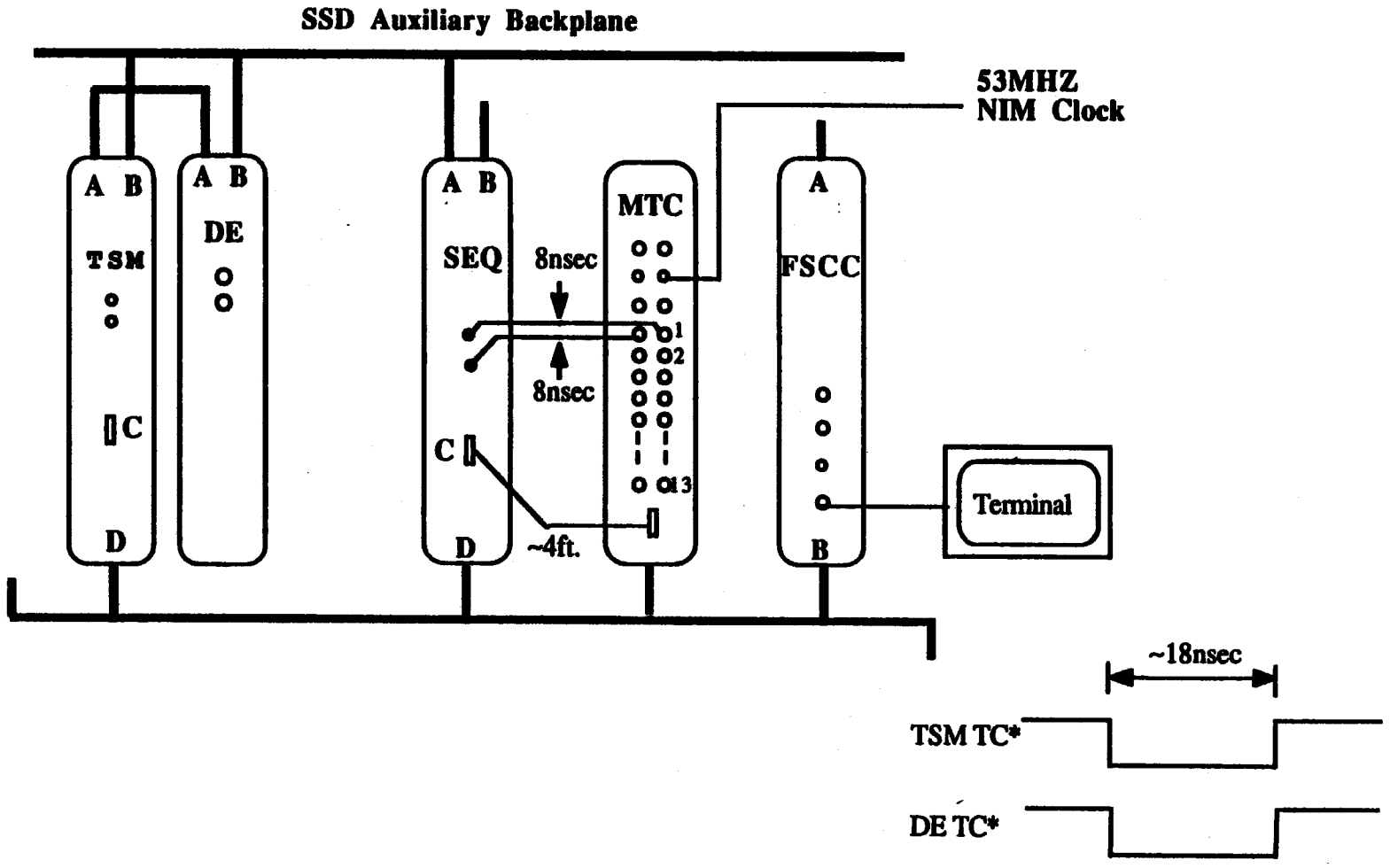


Figure 5: Configuration for SSD Single Channel Readout Test With TSM

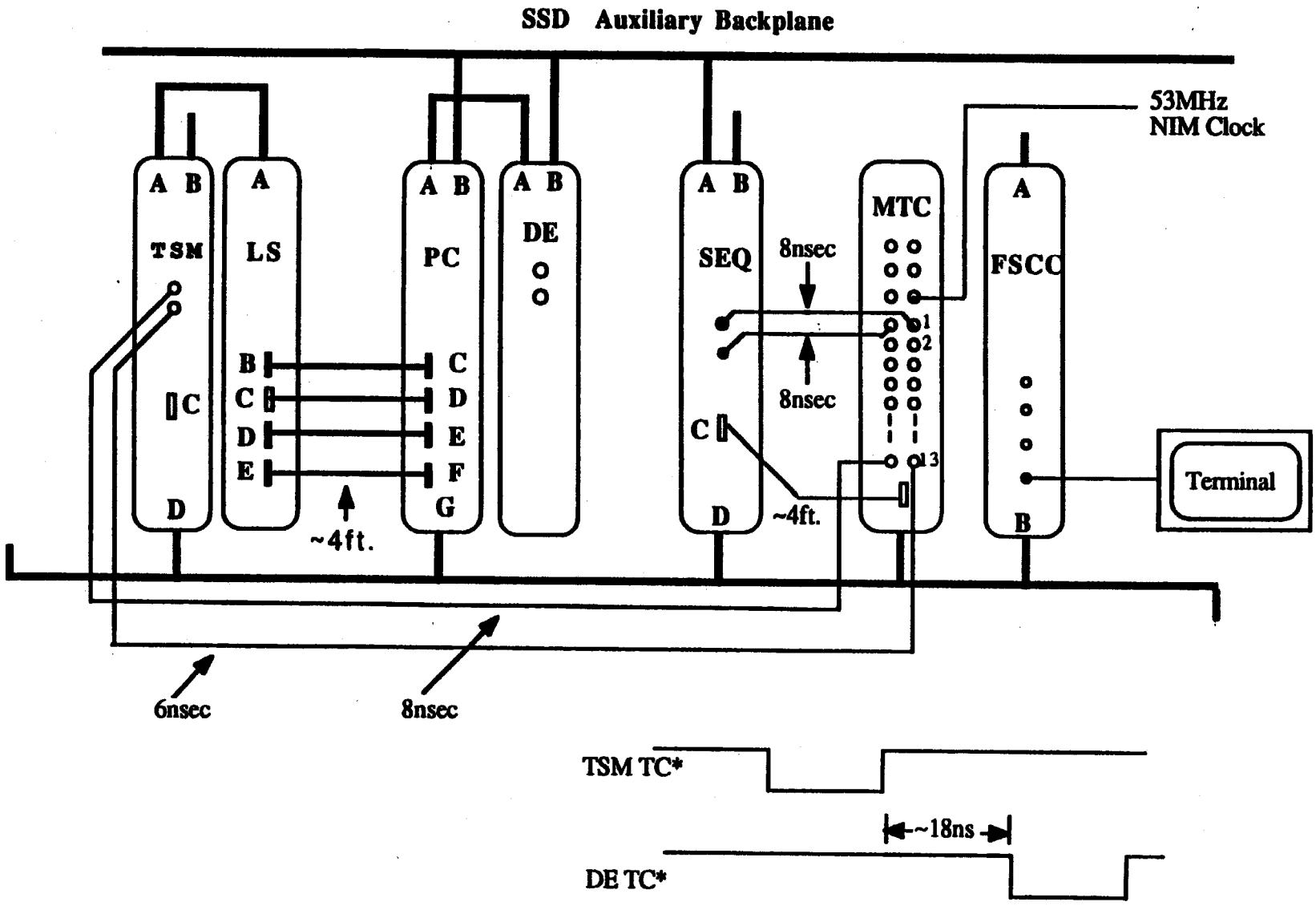


Figure 6: Configuration to Test PC Input Port

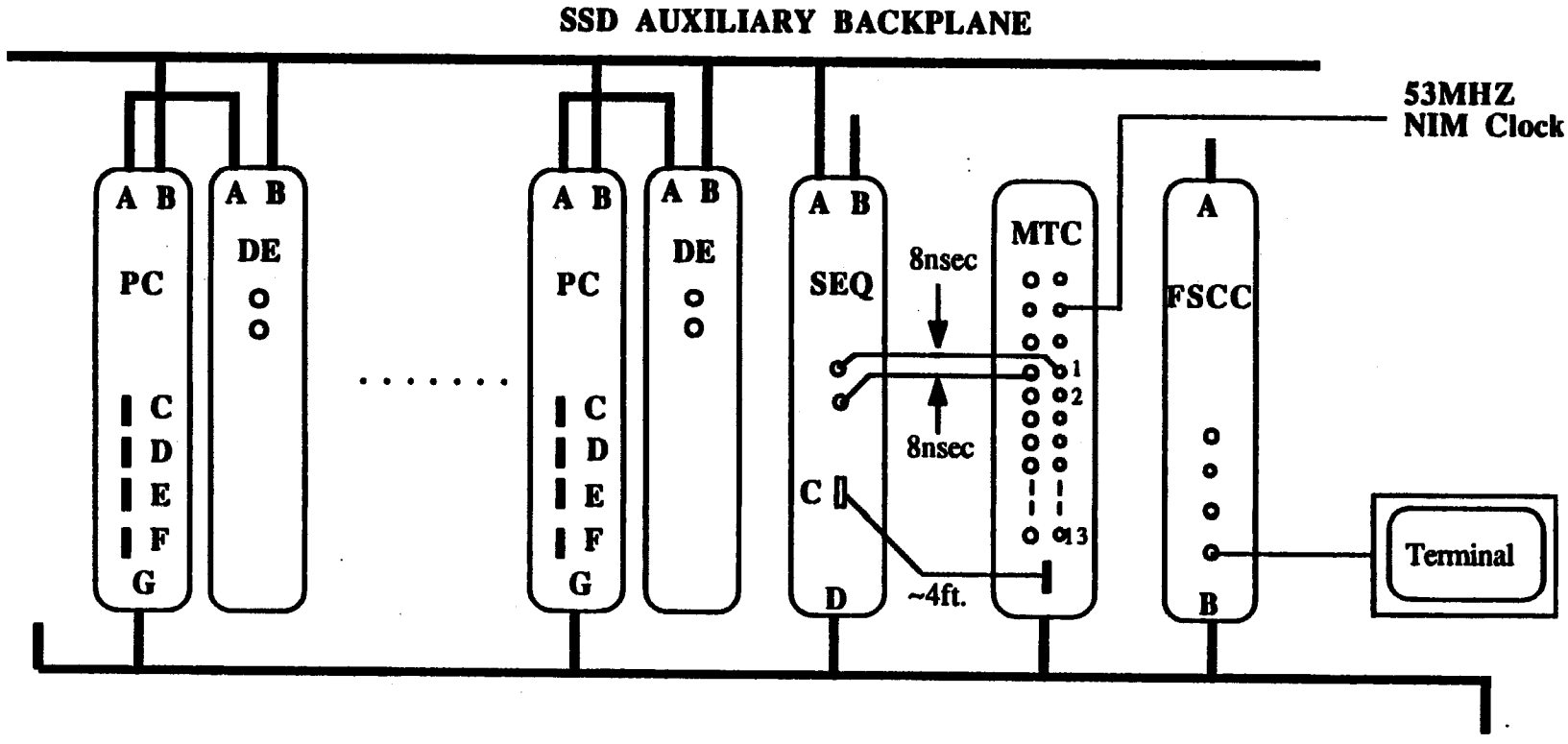


Figure 7: Configuration Test fo SSD Readout Test

Fermi National Accelerator Laboratory

SSD TEST STAND

--PRELIMINARY--

April 2, 1990

Carl Swoboda, Mark Bowden, Dave Christian, Miguel Fachin, Hector Gonzalez
Wolfgang Kowald, Garry Moore, Panayotis Spentzouris

1. GENERAL INFORMATION

The Silicon Strip Detector Readout System will contain hundreds of modules. An automated test stand is required to initially test the integration of each of the modules into a system that operates properly together at the crate level. The techniques and hardware developed for the initial tests will be used to test the production modules as they become available and before they are installed in the field. The Test Stand will also be used after installation into the experiment by support personnel to maintain the system and the modules.

1.1 Purpose

The Test Stand will be used to test the modules used in the Silicon Strip Detector System at the crate level. It is intended to be used as an automated test system to test production quantities of all the modules in the system. The SSD Test Stand is not intended to be a module development station. Each module in the system is assumed to have been fully developed. Typical problems detected in Test Stand tests might be due to failed parts, wrong parts, board solder shorts, etc. Design problems such as signal cross-talk, logic design errors, etc. should have been resolved long before these tests are run. On the other hand, it will be possible to use a special diagnostic module (please see Test Stand Module (TSM) specification) to perform tests on an installed system to help resolve problems that may be out of the ordinary.

1.11 Goals

1. Test modules at the crate/module level
2. Menu driven diagnostics
3. Testing as close as possible to actual system operation
4. Automatic test pattern selection
5. Field use desireable

The Test Stand will be capable of testing the modules that comprise the SSD system together at the crate level. The test will be as close to normal system operation as practical. It will be possible to install a test module in a field installed system to test the modules in an individual crate. Software diagnostics will be menu driven and will be user friendly. The Test Stand must be capable of helping the operator determine if any of the modules in the system are operating properly at the module level.

2. THEORY OF OPERATION AND OPERATING MODES

The Test Stand will require a working module of each type of module since the test is a module substitution technique. The Test Stand is not intended to be a module development station. The use of the Test Stand assumes that the Test Stand has been tested by running the software diagnostics on modules that are known to be good. After that test is complete the module under test can be substituted for the known good module and the tests repeated. This should allow rapid automated testing of each of the system modules in an environment as close as possible to the real system. Errors at the board level will be detected and as much detail as possible will be reported. This of course assumes that the individual modules have error registers that can be read.

2.1 Basic Operation

A block diagram of the Test Stand is shown in Figure 1. The Test Stand Module (TSM), shown shaded in Figure 1, contains a pattern memory, control logic, and a fiberoptic receiver. The FASTBUS Smart Crate Controller (FSCC) will be down-loaded with a test pattern through a RS232 or Ethernet link. The FSCC will load the pattern memory in the TSM with that pattern and start system data acquisition. A simulated trigger signal will be generated that causes the Main Timing Controller (MTC) to generate an event encode address to the Delay/Encoder (D/E). The D/E will encode the pattern and place it into the Sequencer (SEQ) event buffer. The SEQ will also transmit the data over the fiberoptic link to the fiber FIFO in the TSM. The FSCC will then read the SEQ event buffer and the fiber buffer and compare the data to the pattern loaded into the TSM pattern memory. Errors will be reported to the operator.

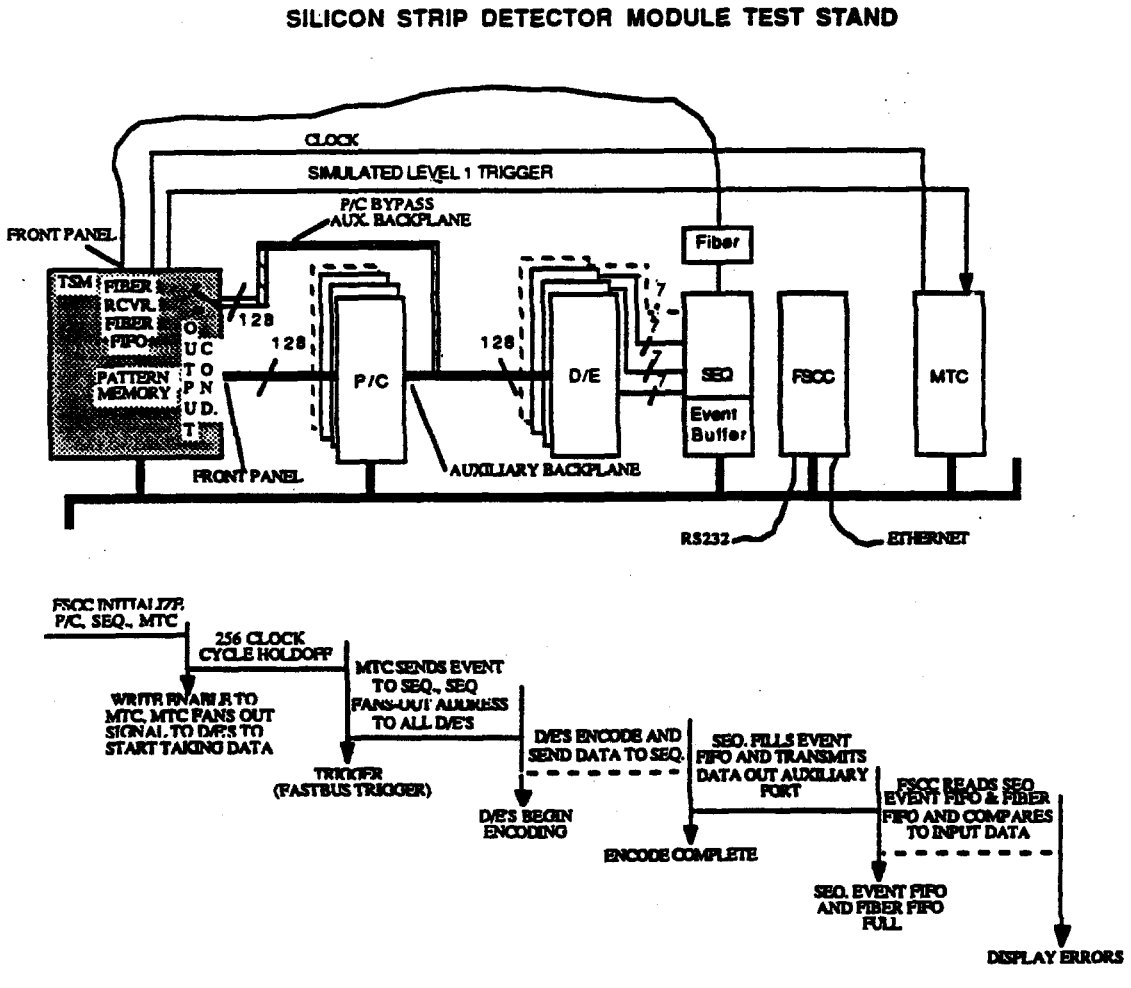


Figure 1; Test Stand Block Diagram

3. SYSTEM SOFTWARE DESCRIPTION

The Test Stand application software will incorporate software that was written for each module during the development stage if possible. Overall system test software requirements are similar to the application programs that must be written for actual system operation. The FSCC will be used as the FASTBUS Master in the Test Stand. The FSCC will be down loaded with a program that will initialize the individual modules in the system, start data acquisition and encoding, and finally compare transmitted hit patterns with those received by the SEQ and the fiberoptic FIFO buffer. Inconsistencies in the received data will be flagged and reported to the operator. The test options and selections will be available from a menu driven display.

The application software must be capable of performing the following operations on the SSD system modules through the FASTBUS interface on the appropropriate modules. The operations listed are basically initialization routines and must be augmented by the software that performs tests on the integrated system.

Test Stand Module

- Write/Read Pattern Memory
- Read Fiberoptic FIFO
- Start Data Acquisition (Simulated Level 1 to MTC)

Master Timing Controller

- Reset
- Write Enable: Start Data Acquisition
- Calibration Mode
- Debug Mode
- Clock Phase Adjust (Programmable Delay)
- Trigger Pipeline Depth
- Read Address Offset
- Errors

Postamp/Comparator

- CSR0
- Run/Halt
- Enable Disable Latches
- Clear Latches
- Enable Sum Channel Latches
- Clear Sum Channel Latches
- Enable/Disable Clock to Diagnostic Counter
- Enable/Disable Clock to D/A(s)
- CSR1
- Data to Diagnostic Counter
- D/A Data (Thresholds)
- Errors

Sequencer

- Write/Read Programmable Delay
- Write/Read Plane/Encoder I.D. RAM
- Write/Read Block/Word Count
- Read Event Buffer
- Errors

3.1 SUGGESTED TESTS TO PERFORM USING THE SSD TEST STAND

INITIALIZATION (Performed by FSCC)
- Postamp/Comparator
- Sequencer
- MTC
- TSM (Pattern Generator)

1. FSCC sends write or read to selected module register
   a. Continuous until stopped by operator.

2. FSCC sends MTC Address/Write Enable/Sync
   a. Continuous until stopped by operator.

3. Input to Postamp/Compartor module from DCC's preamp card.
   a. Input to P/C is a known fixed pattern.
   b. Delay/Encoder encodes pattern.
   c. Sequencer places addresses into event buffer.
   d. Continuous until stopped by operator.

4. FSCC reads event buffer in Sequencer until stopped by oeprator. (empty FIFO ??)

5. FSCC reads event buffer in Sequencer and compares readout with DCC fixed pattern preamp board.

6. FSCC loads pattern into TSM
   a. TSM transmits pattern to Postamp/Comparator.
   b. FSCC reads Sequencer event buffer and compares to pattern loaded into TSM.
   c. FSCC changes pattern in TSM - repeat starting at a.
   d. Continuous until stopped by operator.

FULL CRATE TEST *

7. Tests using Postamp/Comparator pattern generation mode - No TSM required.
   a. Load pattern into P/C.
   b. Start data acquisition.
   c. Read pattern (addresses) from Sequencer event buffer.
   d. Compare Pattern set into P/C to addresses read from Sequencer.
   e. Change pattern loaded into P/C - repeat starting at a.
   f. Change P/C crate address - repeat starting at a.
   g. Continuous until stopped by operator.

* A variation of this test can be used by vendors to test production quantities of the Postamp/Comparator and Delay/Encoder modules.

3.2 Software Approach

INPUT/OUTPUT SPECIFICATIONS

Test Stand Module (TSM)

FASTBUS Interface
128 outputs formatted for output to the Delay/Encoder over the Auxiliary backplane
128 outputs formatted for output to the Postamp/Comparator through the front panel
Fiber Receiver/Driver; four optical inputs, one optical output
Simulated Clock Output
Simulated Level 1 Trigger

Master Timing Controller (MTC)

FASTBUS Interface
Clock Input
System Control as Detailed in MTC Specification

Postamp/Comparator (P/C)

FASTBUS Interface
128 inputs through front panel

Sequencer

FASTBUS Interface
System Control as Detailed in Sequencer Specification

FASTBUS Smart Crate Controller

FASTBUS Interface
RS232
Ethernet

4.1 Communication Interfaces

Communication with the outside world will take place through the RS232 or the Ethernet ports on the FSCC.

5. PHYSICAL SPECIFICATIONS

5.1 Packaging

The Test Stand will will be packaged in FASTBUS .

5.11 Physical Size

5.2 Power Requirements

5.3 Cooling Requirements

5.4 Integrated Circuits Used

5.5 Pin Configurations

APPENDIX A - Info

April 2, 1990
Fermi National Accelerator Laboratory
Computer Division
Data Acquisition Electronics Department

Draft Specification
Fiberoptic Data Transmission Link

Carl Swoboda/Garry Moore
March 21, 1989
Revision A : April 2, 1990

1.0 General Information

1.1 Overview

This fiberoptic data link can be thought of as a general purpose, optically isolated, point-to-point port through which information can be transmitted at relatively high data rates. A commercially available transmitter/receiver chipset, manufactured by Advanced Micro Devices (AMD) and called TAXI, is used. The transmitter chip encodes up to 10 parallel data bits, serializes them, and outputs the result at 125 Mbits/sec. This serial data stream is then fed to an optical transmitter which passes the data through a fiberoptic cable to a remote optical receiver. This optical receiver then converts the optical signal into an electrical bit stream that is applied to the input of the AMD receiver chip. The receiver chip decodes the data, performs a serial-to-parallel conversion, and then outputs the data in parallel along with a strobe which occurs at a data valid point. The result of this operation is the transfer of parallel data over a serial optical link that is basically transparent to the user.

In the Silicon Strip Detector (SSD) application, the fiberoptic data link is configured to transfer data at 50 Mbytes/sec. This rate requires that four individual fiber links be used, each transmitting 10 data bits (a total of 40 bits; 32 bits of data, 8 bits of status), at a rate of 10.42 Mbytes/sec.

1.11 Standard Bus System Used

The SSD readout system is being implemented in the FASTBUS standard. The fiberoptic data link aquires power (+5V) from the FASTBUS crate. Both the optical transmitter and receiver are physically mounted on FASTBUS auxiliary boards but have no physical connection to the FASTBUS backplane.

1.12 Number of Channels

Basically, the fiberoptic data link is a single channel port, connecting a transmitting node to a receiving node operating at a data transfer rate of 41.68 Mbytes/sec. Word width at the transmitting and receiving node is 40 bits (32 bits of data, 8 bits of status).

1.2 Application

The fiberoptic data link is a point-to-point pipelined data mover presently capable of transmitting data at 41.68 Mbytes/sec. Any application that may require data transfers at this rate or higher is a potential customer for this link.

1.3 Packaging

The fiberoptic data link requires no special packaging, and may be implemented in any system that provides the proper voltages. In the SSD case, the transmitting node is packaged on a FASTBUS auxiliary board. The receiving node can be implemented in any appropriate configuration or system capable of accepting 40 bits of parallel data and a strobe every 96 ns.

1.32 Pinout

The connections between the FASTBUS board and the auxiliary board containing the fiberoptic data link components will be as defined in Table I of this specification. The connection to the outside world will be through 5 fiberoptic cable connectors located on the auxiliary backplane board.

Table 1 : Sequencer Module Pin List

(Viewed From Front of Crate-3/7/89)

,Ø1 Clock, Slot 25,23,21	B01-Reset	A01-53MHZ,Ø1 Clock, Slot 13,11,9
,Ø1 Clock, Slot 19,17,15	B02-S0	A02-53MHZ,Ø1 Clock, Slot 7,5,3
ata 0, Slot 24	B03-S1	A03-Hit Data 0, Slot 1
ata 1, Slot 24	B04-S2	A04-Hit Data 1, Slot 1
ata 2, Slot 24	B05-S3	A05-Hit Data 2, Slot 1
ata 3, Slot 24	B06-S5	A06-Hit Data 3, Slot 1
ata 4, Slot 24	B07-LINK ERROR	A07-Hit Data 4, Slot 1
ata 5, Slot 24	B08-SSTROBE	A08-Hit Data 5, Slot 1
ata 6, Slot 24	B09-Sync	A09-Hit Data 6, Slot 1
ata 7, Slot 24	B10-Sync Err	A10-Hit Data 7, Slot 1
Valid, Slot 24	B11-D00	A11-Data Valid, Slot 1
-5.0 Volts	B12-D01	A12-VEE, -5.2 Volts
Data 0, Slot 20	B13-D02	A13-Hit Data 0, Slot 5
Data 1, Slot 20	B14-D03	A14-Hit Data 1, Slot 5
Data 2, Slot 20	B15-D04	A15-Hit Data 2, Slot 5
Data 3, Slot 20	B16-D05	A16-Hit Data 3, Slot 5
Data 4, Slot 20	B17-D06	A17-Hit Data 4, Slot 5
Data 5, Slot 20	B18-D07	A18-Hit Data 5, Slot 5
Data 6, Slot 20	B19-D08	A19-Hit Data 6, Slot 5
ta 7, Slot 20	B20-D09	A20-Hit Data 7, Slot 5
Valid, Slot 20	B21-D10	A21-Data Valid, Slot 5
	B22-D11	A20-GND
Data 0, Slot 16	B23-D12	A23-Hit Data 0, Slot 9
Data 1, Slot 16	B24-D13	A24-Hit Data 1, Slot 9
Data 2, Slot 16	B25-D14	A25-Hit Data 2, Slot 9
Data 3, Slot 16	B26-D15	A26-Hit Data 3, Slot 9
Data 4, Slot 16	B27-D16	A27-Hit Data 4, Slot 9
Data 5, Slot 16	B28-D17	A28-Hit Data 5, Slot 9
Data 6, Slot 16	B29-D18	A29-Hit Data 6, Slot 9
Data 7, Slot 16	B30-D19	A30-Hit Data 7, Slot 9
Valid, Slot 16	B31-D20	A31-Data Valid, Slot 9
	B32-D21	A32-VEE, -5.2 Volts
26 MHZ Clock	B33-D22	A33-Right 26 MHZ Clock
Data 0, Slot 14	B34-D23	A34-Hit Data 0, Slot 11
Data 1, Slot 14	B35-D24	A35-Hit Data 1, Slot 11
Data 2, Slot 14	B36-D25	A36-Hit Data 2, Slot 11
Data 3, Slot 14	B37-D26	A37-Hit Data 3, Slot 11
Data 4, Slot 14	B38-D27	A38-Hit Data 4, Slot 11
Data 5, Slot 14	B39-D28	A39-Hit Data 5, Slot 11
Data 6, Slot 14	B40-D29	A40-Hit Data 6, Slot 11
Data 7, Slot 14	B41-D30	A41-Hit Data 7, Slot 11
Valid, Slot 14	B42-D31	A42-Data Valid, Slot 11
	B43-D32	A43-VCC, +5.0 Volts
Data 0, Slot 18	B44-D33	A44-Hit Data 0, Slot 7
Data 1, Slot 18	B45-D34	A45-Hit Data 1, Slot 7
Data 2, Slot 18	B46-D35	A46-Hit Data 2, Slot 7
Data 3, Slot 18	B47-CLOCK	A47-Hit Data 3, Slot 7
Data 4, Slot 18	B48-Event Address Valid	A48-Hit Data 4, Slot 7
Data 5, Slot 18	B49-Event Address Wrt. En.	A49-Hit Data 5, Slot 7
Data 6, Slot 18	B50-Event Address 0	A50-Hit Data 6, Slot 7
Data 7, Slot 18	B51-Event Address 1	A51-Hit Data 7, Slot 7
Valid, Slot 18	B52-Event Address 2	A52-Data Valid, Slot 7
+5.0 Volts	B53-Event Address 3	A53-GND
Data 0, Slot 22	B54-Event Address 4	A54-Hit Data 0, Slot 3
Data 1, Slot 22	B55-Event Address 5	A55-Hit Data 1, Slot 3
Data 2, Slot 22	B56-Event Address 6	A56-Hit Data 2, Slot 3
Data 3, Slot 22	B57-Event Address 7	A57-Hit Data 3, Slot 3
Data 4, Slot 22	B58-D36	A58-Hit Data 4, Slot 3
Data 5, Slot 22	B59-D37	A59-Hit Data 5, Slot 3
Data 6, Slot 22	B60-D38	A60-Hit Data 6, Slot 3
Data 7, Slot 22	B61-D39	A61-Hit Data 7, Slot 3
Valid, Slot 22	B62-STROBE	A62-Data Valid, Slot 3
-5.2 Volts	B63-ACKNOWLEDGE	A63-GND
Ø,Ø2 Clock, Slot 24,22,20	B64-GND	A64-53MHZ,Ø2 Clock, Slot 11,9,7
Ø,Ø2 Clock, Slot 18,16,14	B65-VTT, -2 Volts	A65-53MHZ,Ø2 Clock, Slot 5,3,1

1.33 N/A

1.4 Power Requirements

The auxiliary card implementation will require the following voltages and currents:

Receiver	+5v @ 1.75A
Transmitter	+5v @ 1.5A

1.41 Control and Monitoring Requirements

The fiberoptic data link uses a simple standard protocol to communicate between transmitting and receiving nodes.

1.5 Cooling Requirements

The fiberoptic data link auxiliary board will be cooled by air passing over the surface of the auxiliary board.

1.6 Unusual Requirements N/A

2.0 Theory of Operation

2.1 Basic Operation

The fiberoptic data link is a data pipeline port through which parallel data is encoded, serialized, and transmitted optically over fiberoptic cable. At the receiving node the data is optically received, converted to electrical signals, decoded, de-serialized and then made available as parallel multi-bit words.

A block diagram of the fiberoptic data link is shown in Figure 1. This description assumes that there is a one-to-one correspondence between the transmitting node and the receiving node. In other words, there is one receiver connected to one transmitter. An alternative arrangement might be to connect multiple transmitting nodes to a single receiving node. In this case a Permit to Transmit is used at each SEQ or FSCC to control the number of nodes transmitting and the data is or'ed optically or electrically at the receiver.

In either case, the fiberoptic data link is operated according to a protocol that defines a very simple communication interchange between a transmitting and receiving node. The protocol does not stipulate a data transfer rate since future implementations of this link will likely be at higher data transfer rates.

The link itself has no intelligence. Data is applied to the link in parallel, received at the remote end, and then presented in parallel as though a multiconductor cable were connecting the two devices.

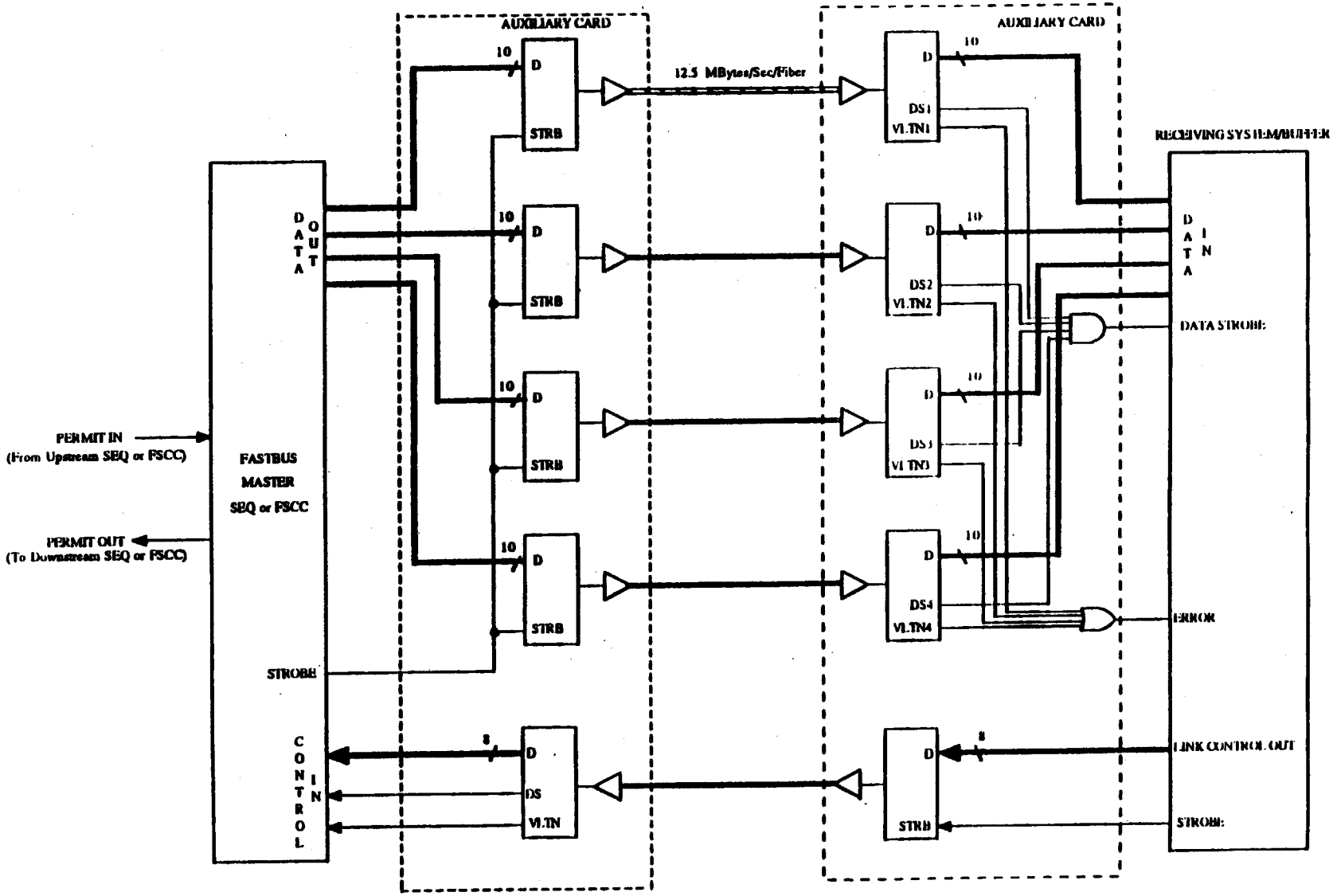


Figure 1; Fiberoptic ink Block Diagram

The fiberoptic data link contains five separate fiberoptic channels, each operating at 10.42 Mbytes/sec. Four of the fibers carry pipeline data and status information to the remote node. The fifth fiber is used to transmit acknowledge or error information from the remote node back to the originating node. The four fibers carrying data to the remote node are operating at an aggregate rate of 41.68 Mbytes/sec, with the acknowledge link operating at 12.5 Mbytes/sec. Commercially available communication chips and optical components are used in the implementation of the link.

Appendix A of this document details the communication chips (AMD TAXI Chips) as well as the optical components used in this implementation.

2.2 N/A

2.3 Addressing Modes

The fiberoptic data link contains no system interface and is therefore not addressable.

2.31 Data Transfer Description and Transfer Rates

The FASTBUS data acquisition system communicates with the fiberoptic link through the FASTBUS auxiliary backplane. A FASTBUS module connects to the link through an auxiliary backplane connector. The fiberoptic data link components are mounted on a FASTBUS auxiliary board that plugs into the auxiliary backplane at the back of a standard FASTBUS crate. The link accepts 40 bit wide (32 bits of data, 8 bits of status) data words and a strobe using TTL logic levels. The FASTBUS transmitting module is responsible for implementing the simple communication protocol as detailed in Appendix A. through the use of the 8 status bits. The module must also supply the link with 32 bits of parallel data and a strobe. The rate of data transfer to the fiberoptic link is controlled by the FASTBUS transmitting module. A maximum rate of transfer between the module and the link is a 40 bit word every 80 ns. The transmitting link has the ability to signal the FASTBUS transmitter that is cannot accept data. This status flag can be used by the module to time the transmissions over the link. The optical receiving node can output a 40 bit data word and strobe at a maximum data rate of one per 80 ns.

An example of a data transfer using the link protocol is shown in Figure 2. The transmitter begins the communication session by transmitting a Start of Message (SOM) control code. The transmitting node waits for an acknowledge transmission from the receiving node for a specific amount of time (timeout protection). If and when the acknowledge signal arrives at the transmitter, data transmission begins. At the end of data an End of Message (EOM) is transmitted to the receiving node. The receiving node acknowledges that it has received the EOM code. Additional data transmissions could follow without waiting for the initial SOM/acknowledge again. The SOM merely tests the integrity of the link before transmitting data.

Figure 2 also contains an example of a communication session in which the receiving node detects an error. In this case an error message is transmitted back to the transmitting node. The transmitting node will continue to transmit data during the time it takes for the receiving node to detect an error and transmit that information back to the transmitting node. When the transmitting node realizes that an error message has arrived, an error handling routine must be activated that resolves the problem based on system level considerations.

3.0 Input/Output Specifications

3.1 Communication Interfaces

This link is in itself a communication port between a transmitting and receiving no implemented in almost any system. The fiberoptic link and a simple data pipeline communicatio.. protocol provides both electrical and logical system isolation. The transmitting node accepts data in parallel, transmits the data, receives the data at the remote node, and makes the data available in parallel as though a muticonductor cable were connected between the two points. This transparency makes the connection of two different systems relatively easy. The "bridge" between different systems is implemented in the design of the transmitting and receiving node interfaces to the fiber link.

3.11 Description and Operation of Ports

The fiberoptic link has a 40 bit (32 bits of data, 8 bits of status) parallel input port at the transmitting node and a 40 bit (32 bits of data, 8 bits of status) parallel output port at the receiving node. The link input port is accessed through a connection between a FASTBUS module and the FASTBUS auxiliary card containing the fiberoptic link components. The link output port will be available for use in any system implementation that is capable of accepting a 40 bit parallel data word.

3.12 Communication Protocol

The communication protocol will be implemented according to the emerging fiberoptic data link standard presently under review by the FASTBUS Standards Committee.

3.2 Analog/Digital Signals

3.21 Logic Levels

Digital signal levels at the input to the optical transmitting node and at the output of the opt.. receiving node are at TTL levels.

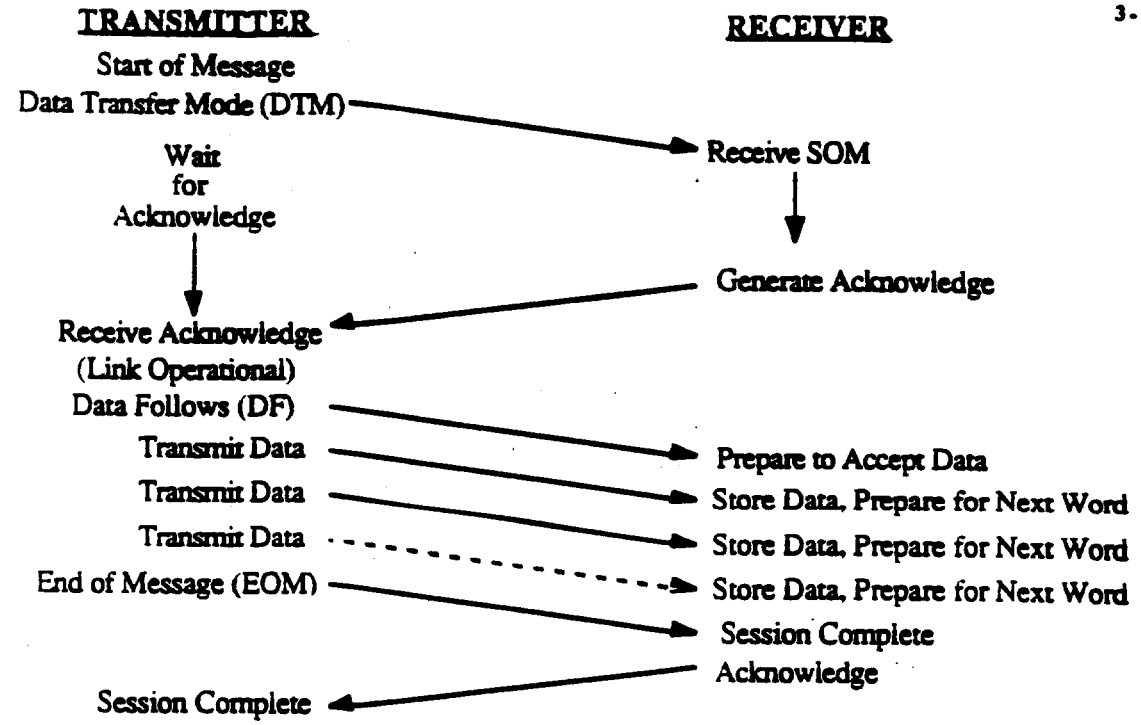
4.0 System Software

4.1 Initialization N/A

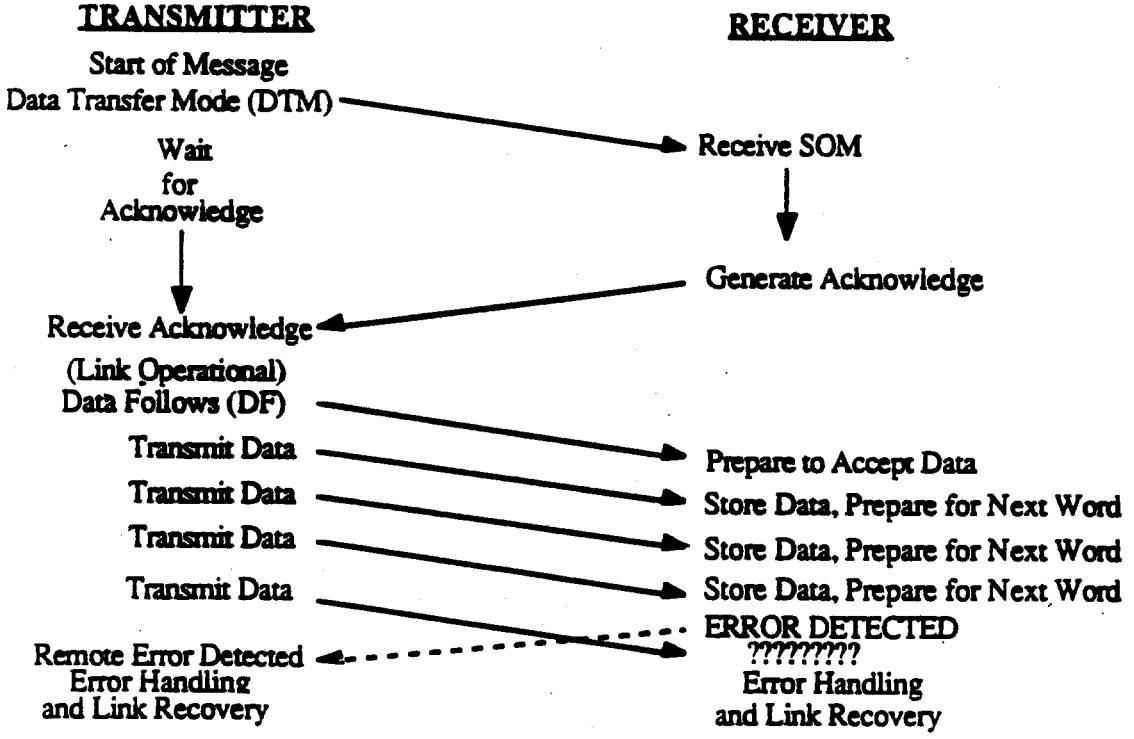
4.2 System Software

Control of the link both at the transmitting and receiving end is the responsibility of the devices to which the link is interfaced. The SSD FASTBUS Smart Crate Controller and/or Sequencer will contain the required link control logic.

COM SESSION
3-13-8



Normal Communication Session



Communication Session With Remote Error Detected

Figure 2: Communication Session Example

PN 434
Version : V1.0
12-Nov-1990

Silicon Strip Detector System Single Board Diagnostic Tests

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+++DRAFT+++

This document describes the diagnostic test software for individual boards in the Silicon Strip Detector (SSD) system.

KEYWORDS: Diagnostic, FASTBUS, SSD, Silicon Strip Detector

Systems Supported: pSOS, VMS V5.3
Software Version:

CONTENTS

CHAPTER 1

SSD SINGLE BOARD TESTS

1.1 INTRODUCTION

The single board tests are a collection of SSD board level diagnostics. Tests are included for the Postamp Comparator (PC), Delay Encoder (DE), Sequencer (SE), and Master Timing Controller (MTC). Each of the tests assume a working FASTBUS Smart Crate Controller (FSCC), and a working SSD FASTBUS crate and power supplies. In addition, some of the tests require special test modules. The purpose of these tests is twofold. First, the tests are intended for initial board qualification; and, second to diagnose and requalify a board that has broken in a previously working SSD system. In the case of a previously working system, it is assumed that a bad board is isolated by substitution or some other system level diagnosis method.

1.2 SINGLE BOARD TEST OPERATION FORMATS

The diagnostic can be run in a variety of ways, but the method with the fastest execution speed and most convenience is using the ROM version of the code. The ROM version of the diagnostic can be installed in FSCC ROM bank 2. (Copies can be made of the latest version in release from Computing Department master prom set.) If FSCC ROM bank 2 is not available, the diagnostic can be downloaded from the SSD_DIAG$tests product directory. Both the ROM version and downloaded version of the diagnostic run in FSCC RAM, so execution speed is the same. Downloading the diagnostic can take up to 10 minutes over a serial line, making this method far less convenient than using the ROM version. The diagnostic may also be run using remote procedure calls, using either the ethernet or serial front panel ports on the FSCC. Although the ethernet version does offer faster execution speed, both methods have relatively slow execution speed. Details of using the ROMed version follows.

1.3 ROM

The following sequence of commands copies the diagnostic code from FSCC ROM bank 2 to FSCC RAM, and starts the diagnostic.

{reset the FSCC manually with the front panel reset button}

```
$ SET HOST/DTE ttnn:          (establish serial communications with FSCC)
pROBE> go 40000               (run EPROM to RAM copy program)
pROBE> gs                     (start pSOS and do other board initializations)
pROBE> go                     (start diagnostic)
```

1.4 ORGANIZATION

The Single Board Tests are organized under a top level menu. Each of the Single Board Tests contain a main menu and submenus. There are also options in the top level menu to provide an interface for tailoring FASTBUS evironment parameters. The top level menu:

```
        SSD Single Board Test Menu
        ==========================
    1) Initialize FASTBUS
    2) Arbitrate (status = xxxx)
    3) Release Bus
    4) Set Long Timer (xxxx usec)
    5) Set Short Timer (xxxx usec)
    6) Set Primary Addresses
    7) Postamp Comparator menu
    8) TSM/Delay Encoder menu
    9) Sequencer menu
   10) Master Timing Controller menu
   11) Select Call mode (mode = Get Menu)
   12) Loop on tests switch (F)
   99) Exit to pROBE
   Enter Command:
```

1.4.1 Initialize FASTBUS

When the Single Board Test diagnostic is started, the FASTBUS environment is automatically initialized by the FASTBUS routines called by this menu option. Each FASTBUS Standard Routine that is part of this initializaion is displayed in a banner above the top level menu. The initialization creates a FASTBUS environment ID that is passed to the module tests, so an error will occur if this menu option is called more than once before calling menu option 3) Release Bus. This FASTBUS initialization routines are:

- GPMINI - initialize interrupts and internal database
- FBOPEN - open FASTBUS routines for use
- FCIENV - allocate an environment ID and associated storage
- FNPALL - allocate FASTBUS port for use
- FBPSET(EG) - set environment parameter to enable geograhic addressing
- FBPSET(COEN) - set environment parameter to enable FSCC data FIFO to processor FIFO copy
- FBPSET(EOBI) - set environment parameter to enable end of block interrupt

1.4.2 Arbitrate

The menu option shows the current arbitor status of the FSCC, one of either "Master", "Slave", or "unknown". If this option is chosen, the FSCC tries to arbitrate for bus mastership using the selected arbitration level. It is not necessary for the FSCC to be bus master to run these tests.

1.4.3 Release Bus

This option will release the bus and delete the current FASTBUS environment ID using the following routines:

- FRLENV
- FBCLOS

1.4.4 Set Long Timer

The menu option displays the current environment value for the long timer. Selecting this option allows the long timer to be set to a new value. After selecting menu item 1) Initialize FASTBUS, the long timer will always be reset to 5000000 usec.

1.4.5 Set Short Timer

Same as above, but the short timer can only be enabled or disabled. Selecting 1500 enables and selecting 0 disables the timer.

1.4.6 Set Primary Address Menu

Set the primary addresses for the SSD modules. The submenu displays the current values of the PADs.

1.4.7 Postamp Comparator Menu

Queries user if 53MHz clock is present. After user [Y/N] response, calls the main menu for the PC tests.

1.4.8 TSM/Delay Encoder Menu

Calls the main menu for the Delay Encoder tests (which use the TSM).

1.4.9 Sequencer Menu

Calls the Sequencer tests main menu.

1.4.10 Master Timing Controller Menu

Calls the Master Timing Controller tests main menu.

1.4.11 Select Call Mode

Allows the call mode for the test to be modified. The call mode currently active is displayed by this menu item. There are four call modes possible, the default mode being to get the main menu of a single board test. The three other call modes include:

- Continue on Error - Tests do not terminate when an error is encountered.

- o Stop on Error - Tests terminate when an error is encountered.

- o Get Menu on Error - Tests terminate when an error is encountered and the appropriate menu is displayed.

Depending on implementation, an error message may or may not be displayed in each of the call modes described above.

1.4.12 Loop On Tests Switch

If this menu item displays (T), any test selected from the top level menu will repeat until a keyboard <Return> is entered. Otherwise, any test selected will execute only once.

1.4.13 Exit To PROBE

In the ROM version, this option will terminate the Single Board Tests with a pROBE break.

CHAPTER 2

POSTAMP COMPARATOR SINGLE BOARD TEST

2.1 INTRODUCTION

PC_TEST is a menu driven software tool capable of effectively testing and/or exercising all FASTBUS accessable circuitry of the PostAmp Comparator module. This software is designed to be used as an integral part of the Single Board Test software package.

2.2 TEST HARDWARE SETUP

The PostAmp Comparator stand-alone tests which are described here require a known working FSCC (Fastbus Smart Crate Controller) located in slot 0 of a functional SSD crate, and a PostAmp Comparator module. The PostAmp Comparator module must be located in a valid PostAmp Comparator slot of the SSD crate. The PostAmp Comparator Primary Address can be verified or changed in the top level menu.

The PostAmp Comparator module test can be executed in either automatic or manual test mode. In automatic mode, the user cannot select individual PostAmp Comparator Test options, but will perform an overall GO/NO-GO test of all FASTBUS circuitry on board the module, displaying errors where appropriate. The features tested using this mode are as follows :

Test All Geographical Addressing Circuitry

Data Space Addressing Mode Response

Response to Multiple CSR Space Addresses

Test All Secondary Addressing Ciruitry

Test the NTA Register

Write/Read Response to Valid NTA Addresses

Oh, 1h, 10h, C0000000 - C00000FF (64 DACs Onboard)

Write/Read Response to Invalid NTA Address

Test the CSR0 Register

Check Module ID

Set/Reset/Read Counter Clock Disable/Enable Bits

Set/Reset/Read Channel Force Zero Disable/Enable Bits

Set/Reset/Read Individual Channel Force Zero Disable/Enable Bits

Set/Reset/Read Mode Halt/Run Bits

Test Functionality of CLK1 On Bit

Write/Read Response to Unused CSR0 Bits

Test the CSR1 Register

Write/Read Test Counter Preset Byte (00 - FF)

Write/Read Response to Unused CSR1 Bits

Test the CSR10 Register

Read Onboard DAC Count

Write Response to Unused CSR10 Bits

Test Write/Read of Onboard DACs

Write/Read All Accessable DACs with FF Pattern

Write/Read All Accessable DACs with 00 Pattern

Write/Read All Accessable DACs with Alternating 55/AA Pattern

Write/Read All Accessable DACs with DAC Address

In manual mode, the PostAmp Comparator Test will be called, displaying the full PC_TEST menuing system, which will be described as follows. This option will also select the default error handling mode (see Chapter 1.3.11 for details). The features tested using this mode are as described above for the automatic mode, except for the added features of allowing the user to write a single DAC location using a user defined value,

read a single DAC location, write/read all accessable DACs with a user defined pattern, and allowing continuous looping of a process of series of processes for oscilloscope based testing.

2.3 PC_TEST MENUING SYSTEM

```
PC_TEST
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      ----->  PC_TEST Main Menu
              -----------------

      -----> 1  Test Geographical Addressing
      -----> 2  Test Secondary Addressing
      -----> 3  Exercise PostAmp Comparator

      -----> 99  Exit PC_TEST Environment

       Enter Menu Option (1 - 3, 99) :
```

In response to the prompt, select an option by typing the option number located to the left. Menu selection errors will be flagged and the user will be prompted to re-enter the required option.

2.3.1 Option 1 Test Geographical Addressing:

```
       ----->  Test Geographical Addressing
               --------------------------

       -----> 1  Define Primary Address
       -----> 2  Address PostAmp Comparator
       -----> 3  Release AS-AK Lock
       -----> 4  Exercise Geographical Addressing

       -----> 99  Exit Geographical Addressing Menu

        Enter Menu Option (1- 4, 99) :
```

In response to the prompt, select an option by typing the option number located to the left. Menu selection errors will be flagged the user will be prompted to re-enter the required option.

2.3.1.1 Option 1 Define Primary Address: -

This option prompts the user to enter a valid slot location for the PostAmp Comparator module. Valid slot numbers are displayed for the user. Invalid slot selections will be flagged and the user will be prompted to re-enter a valid slot number.

2.3.1.2 Option 2 Address PostAmp Comparator: -

This option will attempt to perform a primary address to the specified PostAmp Comparator module. If unsuccessful, the user will be notified.

2.3.1.3 Option 3 Release AS-AK Lock: -

This option will attempt to release the current primary address AS-AK lock. If unsuccessful, the user will be notified.

2.3.1.4 Option 4 Exercise Geographical Addressing: -

This option will fully exercise the primary address circuitry of the PostAmp Comparator module. Situations tested for include response to multiple addresses and response to Data Space Addressing. The user will be notified of all occurring errors.

2.3.1.5 Option 99 Exit Geographical Addressing Menu: -

This option will return the user to the previous menu.

2.3.2 Option 2 Test Secondary Addressing:

```
-----> Test Secondary Addressing
       ------------------------

-----> 1  Test NTA Register
-----> 2  Test CSR 00
-----> 3  Test CSR 01
-----> 4  Test CSR 10
-----> 5  Test DAC Load and Read-back
-----> 6  Exercise Secondary Addressing
```

```
-----> 99  Exit Secondary Addressing Menu

 Enter Menu Option (1 - 6, 99) :
```

In response to the prompt, select an option by typing the option number located to the left. Menu selection errors will be flagged and the user will be prompted to re-enter the required option.

2.3.2.1 Option 1 Test NTA Register: -

```
-----> Test NTA Register
       -----------------

-----> 1  Write to NTA Register
-----> 2  Read from NTA Register
-----> 3  Exercise NTA Register

-----> 99  Exit NTA Register Menu

 Enter Menu Option (1 - 3, 99) :
```

In response to the prompt, select an option by typing the option number located to the left. Menu selection errors will be flagged and the user will be prompted to re-enter the required option.

2.3.2.1.1 Option 1 Write To NTA Register: -

This option will write a user specified value to the PostAmp Comparator NTA register. Valid NTA values are displayed for the user. Invalid NTA entries will be flagged and the user will be prompted to re-enter a valid NTA value. If unsuccessful, the user will be notified.

2.3.2.1.2 Option 2 Read From NTA Register: -

This option will allow the user to view the current value stored in the PostAmp Comparator NTA register. If unsuccessful, the user will be notified.

2.3.2.1.3 Option 3 Exercise NTA Register: -

This option will fully exercise the PostAmp Comparator NTA register. All valid NTA values are tested as well as their boundaries. The user will be notified of all occurring errors.

2.3.2.1.4 Option 99 Exit NTA Register Menu: -

This option will return the user to the previous menu.

2.3.2.2 Option 2 Test CSR 00: -

```
-----> Test CSR 00
       -----------

-----> 1  Set a Specific Bit in CSR 00
-----> 2  Read the Status of a Specific Bit in CSR 00
-----> 3  Read CSR 00
-----> 4  Exercise CSR 00

-----> 99  Exit CSR 00 Menu

 Enter Menu Option (1 - 4, 99) :
```

In response to the prompt, select an option by typing the option number located to the left. Menu selection errors will be flagged and the user will be prompted to re-enter the required option.

2.3.2.2.1 Option 1 Set A Specific Bit In CSR 00: -

```
-----> Write CSR 00
       ------------

-----> 1  Set Test Counter Clock Disable Bit
-----> 2  Set Sum Channel Force Zero Disable Bit
-----> 3  Set Individual Channel Force Zero Disable Bit
-----> 4  Set Mode Halt Bit
-----> 5  Set Test Counter Clock Enable Bit
-----> 6  Set Sum Channel Force Zero Enable Bit
-----> 7  Set Individual Channel Force Zero Enable Bit
-----> 8  Set Mode Run Bit
-----> 9  Write to CSR 00

-----> 99  Exit Write CSR 00 Menu
```

Enter Menu Option (1 - 9, 99) :

In response to the prompt, select an option by typing the option number located to the left. Menu selection errors will be flagged and the user will be prompted to re-enter the required option.

2.3.2.2.1.1 Option 1 Set Test Counter Clock Disable Bit: -

This option will set the Test Counter Clock Disable Bit and reset the Test Counter Clock Enable Bit of the PostAmp Comparator CSR 00 register. The Write to CSR 00 option must be executed for this option to take effect.

2.3.2.2.1.2 Option 2 Set Sum Channel Force Zero Disable Bit: -

This option will set the Sum Channel Force Zero Disable Bit and reset the Sum Channel Force Zero Enable Bit of the PostAmp Comparator CSR 00 register. The Write to CSR 00 option must be executed for this option to take effect.

2.3.2.2.1.3 Option 3 Set Individual Channel Force Zero Disable Bit: -

This option will set the Individual Channel Force Zero Disable Bit and reset the Individual Channel Force Zero Enable Bit of the PostAmp Comparator CSR 00 register. The Write to CSR 00 option must be executed for this option to take effect.

2.3.2.2.1.4 Option 4 Set Mode Halt Bit: -

This option will set the Mode Halt Bit and reset the Mode Run Bit of the PostAmp Comparator CSR 00 register. The Write to CSR 00 option must be executed for this option to take effect.

2.3.2.2.1.5 Option 5 Set Test Counter Clock Enable Bit: -

This option will set the Test Counter Clock Enable Bit and reset the Test Counter Clock Disable Bit of the PostAmp Comparator CSR 00 register. The Write to CSR 00 option must be executed for this option to take effect.

2.3.2.2.1.6 Option 6 Set Sum Channel Force Zero Enable Bit: -

This option will set the Sum Channel Force Zero Enable Bit and reset the Sum Channel Force Zero Disable Bit of the PostAmp Comparator CSR 00 register. The Write to CSR 00 option must be executed for this option to take effect.

2.3.2.2.1.7 Option 7 Set Individual Channel Force Zero Enable Bit: -

This option will set the Individual Channel Force Zero Enable Bit and reset the Individual Channel Force Zero Disable Bit of the PostAmp Comparator CSR 00 register. The Write to CSR 00 option must be executed for this option to take effect.

2.3.2.2.1.8 Option 8 Set Mode Run Bit: -

This option will set the Mode Run Bit and reset the Mode Halt Bit of the PostAmp Comparator CSR 00 register. The Write to CSR 00 option must be executed for this option to take effect.

2.3.2.2.1.9 Option 9 Write To CSR 00: -

This option will write a user specified value (as specified by the above enable/disable bit manipulations) to the PostAmp Comaparator CSR 00 register. If unsuccessful, the user will be notified.

2.3.2.2.1.10 Option 99 Exit Write CSR 00 Menu: -

This option will return the user to the previous menu.

2.3.2.2.2 Option 2 Read The Status Of A Specific Bit In CSR 00:

-----> Read CSR 00

-----> 1 Read Module ID Bits
-----> 2 Read CLK1 On Bit
-----> 3 Read Test Counter Enable/Disable Bit
-----> 4 Read Sum Channel Enable/Disable Bit
-----> 5 Read Individual Channel Enable/Disable Bit
-----> 6 Read Mode Run/Halt Bit

-----> 99 Exit Read CSR 00 Menu

Enter Menu Option (1 - 6, 99) :

In response to the prompt, select an option by typing the option number located to the left. Menu selection errors will be flagged and the user will be prompted to re-enter the required option.

2.3.2.2.2.1 Option 1 Read Module ID Bits: -

This option will allow the user to view the current Module ID value stored in the PostAmp Comparator CSR 00 register. If unsuccessful, the user will be notified.

2.3.2.2.2.2 Option 2 Read CLK1 On Bit: -

This option will allow the user to view the current status of the CLK1 On Bit stored in the PostAmp Comparator CSR 00 register. If unsuccessful, the user will be notified.

2.3.2.2.2.3 Option 3 Read Test Counter Enable/Disable Bit: -

This option will allow the user to view the current status of the Test Counter Enable/Disable Bit stored in the PostAmp Comparator CSR 00 register. If unsuccessful, the user will be notified.

2.3.2.2.2.4 Option 4 Read Sum Channel Enable/Disable Bit: -

This option will allow the user to view the current status of the Sum Channel Enable/Disable Bit stored in the PostAmp Comparator CSR 00 register. If unsuccessful, the user will be notified.

2.3.2.2.2.5 Option 5 Read Individual Channel Enable/Disable Bit:
This option will allow the user to view the current status of the Individual Channel Enable/Disable Bit stored in the PostAmp Comparator CSR 00 register. If unsuccessful, the user will be notified.

2.3.2.2.2.6 Option 6 Read Mode Run/Halt Bit: -

This option will allow the user to view the current status of the Mode Run/Halt Bit stored in the PostAmp Comparator CSR 00 register. If unsuccessful, the user will be notified.

2.3.2.2.2.7 Option 99 Exit Read CSR 00 Menu: -

This option will return the user to the previous menu.

2.3.2.2.3 Option 3 Read CSR 00: -

This option will allow the user to view the current value stored in the PostAmp Comparator CSR 00 register. If unsuccessful, the user will be notified.

2.3.2.2.4 Option 4 Exercise CSR 00: -

This option will fully exercise the CSR 00 register circuitry of the PostAmp Comparator module utilizing test sequences from the above menu options. The user will be notified of all occurring errors.

2.3.2.2.5 Option 99 Exit CSR 00 Menu: -

This option will return the user to the previous menu.

2.3.2.3 Option 3 Test CSR 01: -

```
-----> Test CSR 01
       -----------

-----> 1  Set Test Counter Byte in CSR 01
-----> 2  Read Test Counter Byte in CSR 01
-----> 3  Read CSR 01
-----> 4  Exercise CSR 01

-----> 99  Exit CSR 01 Menu

 Enter Menu Option (1 - 4, 99) :
```

In response to the prompt, select an option by typing the option number located to the left. Menu selection errors will be flagged and the user will be prompted to re-enter the required option.

2.3.2.3.1 Option 1 Set Test Counter Byte In CSR 01: -

This option will write a user specified value to the PostAmp Comparator CSR 01 register. Valid Test Counter values are displayed for the user. Invalid Test Counter entries will e flagged and the user will be prompted to re-enter a valid Test Counter value. If unsuccessful, the user will be notified.

2.3.2.3.2 Option 2 Read Test Counter Byte In CSR 01: -

This option will allow the user to view the current Test Counter Byte value stored in the PostAmp Comparator CSR 01 register. If unsuccessful, the user will be notified.

2.3.2.3.3 Option 3 Read CSR 01: -

This option will allow the user to view the current value stored in the PostAmp Comparator CSR 01 register. If unsuccessful, the user will be notified.

2.3.2.3.4 Option 4 Exercise CSR 01: -

This option will fully exercise the CSR 01 register circuitry of the PostAmp Comparator module utilizing test sequences from the above menu options. The user will be notified of all occurring errors.

2.3.2.3.5 Option 99 Exit CSR 01 Menu: -

This option will return the user to the previous menu.

2.3.2.4 Option 4 Test CSR 10: -

-----> Test CSR 10

```
-----> 1  Read CSR 10
-----> 2  Exercise CSR 10

-----> 99  Exit CSR 10 Menu

 Enter Menu Option (1 - 2, 99) :
```

In response to the prompt, select an option by typing the option number located to the left. Menu selection errors will be flagged and the user will be prompted to re-enter the required option.

2.3.2.4.1 Option 1 Read CSR 10: -

This option will allow the user to view the current value stored in the PostAmp Comparator CSR 10 register. If unsuccessful, the user will be notified.

2.3.2.4.2 Option 2 Exercise CSR 10: -

This option will fully exercise the CSR 10 register circuitry of the PostAmp Comparator module utilizing test sequences from the above menu options. The user will be notified of all occurring errors.

2.3.2.4.3 Option 99 Exit CSR 10 Menu: -

This option will return the user to the previous menu.

2.3.2.5 Option 5 Test DAC Load And Read-back: -

```
-----> Test DACs/ADCs
       --------------

-----> 1  Load User Selected DAC
-----> 2  Load all DACs to Full Scale
-----> 3  Load all DACs to Zero
-----> 4  Load all DACs to User Selected Value
-----> 5  Load all DACs, Alternating AA and 55 Values
-----> 6  Load all DACs to Their Corressponding Address
-----> 7  Read User Selected ADC
-----> 8  Read all ADCs
-----> 9  Exercise DACs/ADCs
```

```
-----> 99  Exit Test DACs/ADCs Menu

Enter Menu Option (1 - 9, 99) :
```

In response to the prompt, select an option by typing the option number located to the left. Menu selection errors will be flagged and the user will be prompted to re-enter the required option.

2.3.2.5.1 Option 1 Load User Selected DAC: -

This option will write a user specified value to a user specified DAC location on the PostAmp Comparator module. The Mode Halt Bit located in CSR 00 is temporarily enabled for this option. Valid DAC locations and acceptable DAC values are displayed for the user. Invalid DAC locations and/or unacceptable DAC values will be flagged and the user will be prompted to re-enter valid DAC locations and/or DAC values. If unsuccessful, the user will be notified.

2.3.2.5.2 Option 2 Load All DACs To Full Scale: -

This option will write a Full Scale value to all available DACs on the PostAmp Comparator module. The Mode Halt Bit located in CSR 00 is temporarily enabled for this option. If unsuccessful, the user will be notified.

2.3.2.5.3 Option 3 Load All DACs To Zero: -

This option will write a Zero value to all available DACs on the PostAmp Comparator module. The Mode Halt Bit located in CSR 00 is temporarily enabled for this option. If unsuccessful, the user will be notified.

2.3.2.5.4 Option 4 Load All DACs To User Selected Value: -

This option will write a user specified value to all available DACs on the PostAmp Comparator module. The Mode Halt Bit located in CSR 00 is temporarily enabled for this option. Acceptable DAC values are displayed for the user. Unacceptable DAC values will be flagged and the user will be prompted to re-enter valid DAC values. If unsuccessful, the user will be notified.

2.3.2.5.5 Option 5 Load All DACs, Alternating AA And 55 Values:
This option will write an alternating pattern of AA and 55 values to all available DACs on the PostAmp Comparator module. The Mode Halt Bit located in CSR 00 is temporarily enabled for this option. If unsuccessful, the user will be notified.

2.3.2.5.6 Option 6 Load All DACs To Their Corresponding Address:
This option will write to a valid DAC, that DAC's corresponding address. As an example, the DAC residing at address 7F will be loaded with the value 7F. The Mode Halt Bit located in CSR 00 is temporarily enabled for this option. If unsuccessful, the user will be notified.

2.3.2.5.7 Option 7 Read User Selected ADC: -

This option will allow the user to view the current value of a user specified ADC location on the PostAmp Comparator module. The Mode Halt Bit located in CSR 00 is temporarily enabled for this option. If unsuccessful, the user will be notified.

2.3.2.5.8 Option 8 Read All ADCs: -

This option will allow the user to determine that all available ADCs return the expected values previously stored in all the available DACs located on the PostAmp Comparator module. The Mode Halt Bit located in CSR 00 is temporarily enabled for this option. All DAC/ADC pairs are compared allowing a tolerance of +- 1 bit and displaying any discrepencies. If unsuccessful, the user will be notified.

2.3.2.5.9 Option 9 Exercise DACs/ADCs: -

This option will fully exercise all circuitry associated with addressing, reading and writing the PostAmp Comparator DACs and ADCs, utilizing test sequences from the above menu options. The user will be notified of all occurring errors.

2.3.2.5.10 Option 99 Exit Test DACs/ADCs Menu: -

This option will return the user to the previous menu.

2.3.2.6 Option 6 Exercise Secondary Addressing: -

This option will fully exercise the secondary address circuitry of the PostAmp Comparator module utilizing test sequences from the above menu options. The user will be notified of all occurring errors.

2.3.2.7 Option 99 Exit Secondary Addressing Menu: -

This option will return the user to the previous menu.

2.3.3 Option 3 Exercise PostAmp Comparator:

This option will fully exercise all FASTBUS accessable circuitry of the PostAmp Comparator module including all geographical address, secondary address, and DAC/ADC circuitry. The user will be notified of all occurring errors.

2.3.4 Conclusion

The purpose of this software package is to effectively and efficiently test and exercise all FASTBUS accessable circuitry of the PostAmp Comparator module. The user is alerted to any and all errors which may occur during execution of the test software, allowing further investigation of problem areas.

Questions and/or comments concerning these PostAmp Comparator tests should be forwarded to :

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CHAPTER 3

DELAY ENCODER SINGLE BOARD TEST

3.1 INTRODUCTION

The routine DE_TEST is designed to test the Delay Encoder FASTBUS board of the SSD system using the Test Stand Module (TSM). The paramaters are : the primary address of the TSM, the environemnt identification for the FASTBUS standard routines and a flag, which determines in which mode the routine is called. The routine is written in C and uses MCC8K and VAXC for conditional compilations.

3.2 TEST SETUP

The TSM is used either in a system test, in which it replaces a PC or in a single module test, in which only the DE is tested. In the latter case the TSM controls the DE system signals and is used for the readout of the hits. The format of these hits are different from the ones, which are received from the SE in the system test. This program is designed for the single module test of the DE using the TSM.

The Test Setup is as follows :

- Standard FASTBUS crate and an FSCC in slot 0
- DE
- TSM
- Jumper cards for the auxilliary backplane between DE slot and TSM slot
- Terminating card in slot 13
- Jumper cables on the TSM : J1 - J4 (clock) and J2 - J3 (sync)

3.3 PACKAGES USED

The program uses the following software packages:

- o TSMF.C
- o BUFFER.C
- o FASTBUS standard routines
- o Standard C libraries

3.4 INCLUDE FILES USED

- o Standard C : stdlib.h,math.h,stdio.h
- o FASTBUS : fbpars.h,fberrs.h,fbconstants.h
- o FSCC specific : fscc_ad.h
- o SSD specific : menu_intf.h,tsmreg.h,syst.h

3.5 FEATURES TESTED

The routine DE_TEST tests the full functionality of the DE board. Certain kinds of errors will only be detected, if certain hit patterns are used. One option in the manual menu lets you choose specific patterns. By default, the programm wil generate random patterns.

The test relies on a working TSM board. There is the possibilty to verify the stored data in the TSM memory. TSM.

3.6 SOFTWARE ORGANIZATION

The file DE_TEST.C contains three routines. The main entry point DE_TEST(...) and three support routines, DE_MAKE_HIT_LIST(...), DE_COMPARE_HIT_LIST(...) and DE_PRINT_MENU(). All four routines use global variables. These global variables all start with DE_ and are in capital letters. These variables are initialized at program load time. So if you change variables using the menu option, these changes

are permanent and will be used when the automatic test is called. The seed value for the random number generation is one of the global variables.

3.7 USER GUIDE

The routine DE_TEST can be called in the following modes :

- GO_ON_ERR : An internal buffer is filled with random hits (20 hits in even and 60 hits in odd location). The buffer is organized to reflect the ring buffer located in the DE (0..255). The TSM memory is filled and the TSM transfers to the DE started. The readout loops over all trigger addresses, reads the encoded hits via the TSM and compares it with the generated list of hits. The program does not stop if an error occurs. No error messages are printed. The return value is the number of errors detected. The internal loop counter is set to 10. At every iteration, new random hits are generated.

- STOP_ON_ERR : The steps are the same as above, but if an error occurs, the program will return with a non zero return value, after the first attempt to read an event at trigger address 1. No error messages are printed.

- GET_MENU_ON_ERR : Instead of returning with a non zero return value after detecting an error, the program calls the Menu and waits for commands.

- GET_MENU : In this mode, the Menu is called. No actions are taken. So the buffer is still empty and no FASTBUS operations are performed. The user has full control over the sequence of operations. Error messages will be displayed.

3.7.1 Error Messages

Errors can occur during FASTBUS operations, verification of buffer contents and comparing the predicted hit list with the one received from the TSM.

Errors during FASTBUS operations are reported only if the routine is called in the mode GET_MENU. If verifying the TSM contents gives an error, the local buffer is printed together with the data received from the TSM. If an error is detected during readout, the following error information is given :

```
DE_ERROR : 1, ITERATION : 1, DE_NHIT : 86, LOOP : 0
```

```
   byte          F E D C B A 9 8 7 6 5 4 3 2 1 0
   PBA (000) : 5b01000a0a08022000001039400020 00
    TA (001) : 31c8bf1bfffffedf83c01ffa40f8bfe4
| DE  EXP | DE  EXP | DE  EXP | DE  EXP | DE  EXP | DE  EXP
| yif yif | yif yif | yif yif | yif yif | yif yif | yif yif
* 000 020 * 000 050 * 000 060 * 000 070 * 000 100 * 000 110
* 000 120 * 000 130 * 000 140 * 000 151 * 000 170 * 000 230
* 000 240 * 000 250 * 000 260 * 000 270 * 000 361 * 000 401
* 000 410 * 000 431 * 000 441 * 000 451 * 000 460 * 000 470
* 000 500 * 000 510 * 000 520 * 000 530 * 000 541 * 000 660
* 000 670 * 000 700 * 000 710 * 000 770 * 000 800 * 000 810
* 000 820 * 000 830 * 000 840 * 000 851 * 000 860 * 000 870
* 000 911 * 000 920 * 000 930 * 000 940 * 000 950 * 000 960
* 000 970 * 000 a00 * 000 a10 * 000 a20 * 000 a31 * 000 a40
* 000 a50 * 000 a60 * 000 a70 * 000 b00 * 000 b11 * 000 b20
* 000 b31 * 000 b40 * 000 b50 * 000 b60 * 000 b70 * 000 c00
* 000 c11 * 000 c31 * 000 c40 * 000 d00 * 000 d10 * 000 d20
* 000 d30 * 000 d40 * 000 d50 * 000 d70 * 000 e01 * 000 e30
* 000 e60 * 000 e70 * 000 f01 * 000 f11 * 000 f31 * 000 f41
* 000 f50 * 000 f61

PBA : Previous Bucket Address
TA  : Trigger Address
DE  : data received from the TSM
EXP : data expected
f   : RF flag (Previous Bucket Flag)
y   : Byte number (0..f)
i   : Bit number  (0..7)

(The star indicates that this hit was not found in the received list)
```

The current implementation verifies, that all hits predicted are actually present in the received hit list. It will flag extra hits too.

3.7.2 MAIN MENU

```
 ***** WARNING : Buffer not filled ***** : use l) first
----- DE/TSM Test Menu -----
     a) Set Readout delay (0 [msec])
     b) Initialize TSM, fill event memory and verify
     c) Select Trigger Address (1) and read
     d) Loop over all trigger addresses
     e) Random fill and loop over all trigger addresses
     f) Set maximum error count (10)
     g) Set number of hits (even:20,odd:60) and fill buffer
     h) Print this text          i) Read buffer from file
     j) Write buffer to file     k) Accept hits from PBA (T)
     l) Generate new random buffer and do b
```

```
     m) Set loop counter for c,d and e (10)
     n) Modify buffer              o) Print buffer contents
     p) Toggel menu print out      q) FIFO block transfer enable (T)
     r) Print Error Buffer         s) Clear Error Buffer
     t) Set Trigger Address Correction (0)
     u) Clear Write                v) Verify TSM memory
     z) Scramble buffer(S->J)      w) Unscramble buffer (J->S)
     x) Exit Test (Last Iteration count : 0, Errors : 0)
Enter command ( HELP : h ) :
```

3.7.2.1 Item A) -

You can introduce a delay between iterations.

3.7.2.2 Item B) -

TSM_FILL in TSMF is called. Reset TSM, copy the event buffer to the TSM and read the buffer back in order to verify it. Only the processor controlled block transfers are used. If the block transfer via the FIFO is enabled, it will be disabled before reading and enabled after reading.

3.7.2.3 Item C) -

You can select a specific trigger address and the encoded hit data will be compared to the predicted list of hits. The number of times this operation is executed can be set in item m). The loop can be interrupted by pressing any key of the kerboard.

3.7.2.4 Item D) -

Similar to c), but the routine loops over all trigger addresses, starting with 1 and ending with 0. The number of times this operation is executed, can be set in item m). The loop can be interrupted by pressing any key of the keyboard.

3.7.2.5 Item E) -

The buffer is filled with a random pattern. The number of hits can be selected in item g). The program loops over all trigger addresses. After each loop, the buffer is filled with new random hits.

3.7.2.6 Item F) -

Set the maximum number of errors. The program will stop if the number of errors reaches this maximum.

3.7.2.7 Item G) -

Set the number of hits for random filling. The number of hits for even addresses and odd addresses seperately will be set, the buffer filled and copied to the TSM.

3.7.2.8 Item H) -

The menu is printed.

3.7.2.9 Item I) -

Instead of filling buffers with random numbers or specific patterns, you can read a prepared buffer from a file. This is only useful, if the program runs on the VAX, communicating with the FSCC via Remote Procedure Execution (RPX). When running on the FSCC, the input will be via the serial line.

3.7.2.10 Item J) -

Writes the current buffer to a file. See Item i)

3.7.2.11 Item K) -

This determins, whether hits in the previous bucket (trigger address - 1) will be accepted for the generation of the hit data. Jumpers on the DE must be set accordingly. By default hits in the previous bucket will be accepted.

3.7.2.12 Item L) -

Generate new random buffer, fill the TSM and verify.

3.7.2.13 Item M) -

Set the outer loop counter for c), d) and e). If a key on the keyboard is pressed, the loop is aborted.

3.7.2.14 Item N) -

This option calls a submenu for the filling of the buffer. This submenu is part of the package BUFFER.C.

```
 0  : fill selected position
 1  : fill with row of pattern
 2  : fill with 5555...
                AAAA...
 3  : fill with FFFF...
                0000...
 4  : fill with PC counter -fixed- pattern
 5  : fill with PC counter -running- pattern
 6  : fill with random pattern
 7  : fill with repeated N raw pattern
                LLLL...
                WWWW...
                KKKK...
 8  : display selected positions
 99 : exit
```

3.7.2.15 Item O) -

Output the contents of the buffer at a certain address.

3.7.2.16 Item P) -

En/disable the printout of the menu.

3.7.2.17 Item Q) -

Change the FASTBUS environment to en/disable the block transfer read via the FSCC fifo. Block transfers via the FIFO are enabled by default.

3.7.2.18 Item R) -

Print the error buffer. A circular buffer accumulates the last 20 data errors.

```
Error : 1 , Iteration : 1 , NHIT : 86
  byte          F E D C B A 9 8 7 6 5 4 3 2 1 0
  PBA (000) : 5b01000a0a08022000001039400020 00
   TA (001) : 31c8bf1bfffffedf83c01ffa40f8bfe4
-------------------------------------------------------
Error : 0 , Iteration : 0 , NHIT : 0
  byte          F E D C B A 9 8 7 6 5 4 3 2 1 0
  PBA (000) : 00000000000000000000000000000000
   TA (000) : 00000000000000000000000000000000
```

3.7.2.19 Item S) -

Clear the error buffer.

3.7.2.20 Item T) -

Define an offset from the selected trigger address, which will be subtracted from the trigger address and sent to the TSM. This allows for non synchronized transfers of hits to the DE.

3.7.2.21 Item X) -

Exit the menu and return to the main program.

3.7.2.22 Typical Session -

The following is a typical sequence of events, which is necessary to do the test manually with random hits:

- o Set readout delay a)
- o Set maximum number of errors f)
- o Set maximum loop count m)
- o Set number of hits g)

- Start readout loop e)

The test will be aborted in the following cases:

- The maximum loop count is reached
- The maximum error count is reached
- The user hits a key on the keyboard